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Analysis and Modeling of a Five- Level Inverter

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Abstract:
Multilevel inverters are mainly used in high power applications, where they have proved to be reliable and robust. They operate with low frequency and present high efficiency. Current demand on different reliable, efficient and robust inverters for different energy system has extended multilevel application to small power system as well. In this project, an inverting system will be developed using the cascaded H-bridge multilevel inverter technology, which is able to synthesize a desired ac voltage from several levels of dc Voltages. Multilevel inverter as compared to single level inverters have advantages like minimum harmonic distortion, reduced EMI/RFI generation and can operate on several voltage levels. A multi-stage inverter is being utilized for multipurpose applications, such as active power filters, and in many renewable energy power applications. The PWM signal thus generated is then used as triggering pulses for the multilevel inverters. This Project aims at the simulation study of single phase cascaded H- bridge multilevel inverter using DC voltages MATLAB software. It will be used to investigate and verify the quality of the ac output voltage, harmonic content of the output voltage and effects of different switching scheme.

Keywords: Cascaded H-bridge inverter, PWM, THD, Modified five level inverter

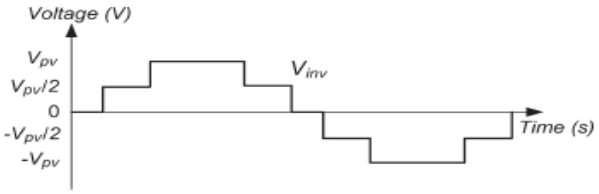
1. Introduction

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application [1-5].

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregates these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depend only upon the rating of the dc voltage sources to which they are connected.

2. Multilevel Inverter

The inverters which produce which produce an output voltage or a current with levels either 0 or +- V are known as two level inverters. In high-power and high-voltage applications these two-level inverters however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. This is where multilevel inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase power rating. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformers or series- connected synchronized-switching devices.



Multilevel inverters generate a staircase waveform. By increasing the number of output levels, the output voltages have more steps and harmonic content on the output voltage and the THD values are reduced. Therefore, they produce high quality output voltage by increasing the number of levels. Different topologies available in multilevel inverters are as follows.

1. Diode Clamped Multilevel Inverter
2. Capacitor Clamped Multilevel Inverter
3. Cascaded H-Bridge Multilevel Inverter

A cascaded multilevel inverter consists of a series of H-bridge (single- phase full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, which may obtain from batteries, fuel cells, or solar cells. Fig. 1 shows a single-phase structure of a cascade inverter with separate dc sources. Each separate dc source is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and –Vdc.

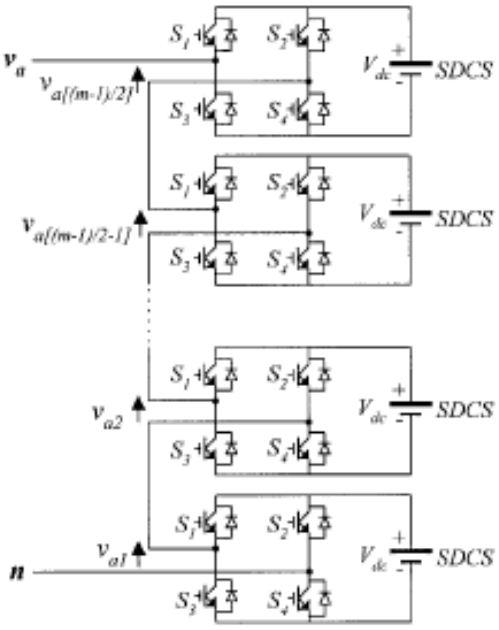


Fig. 1 A single-phase structure of a cascade inverter with separate dc sources

The ac outputs of the inverters are connected in series such that the synthesized voltage waveform is the sum of the inverters outputs. The output phase voltage levels are defined by m = 2s+1, s = no. of dc sources.

Cascaded H-bridge Multilevel Inverter has been receiving wide attention due to its numerous advantages as a dc/ac interface. The number of levels in the output phase voltage and line voltage are 2s+1 and 4s+1 respectively, where s is the number of H-bridges used per phase. For example, Three H- Bridges, Five H-bridge and seven H-bridge per phase are required for 7-level, 11-level and 15-level multilevel inverter respectively. The magnitude of the ac output phase voltage is the sum of the voltages produced by H-bridges [6-9].

Table 1: Comparison between Different Level Inverter Topologies

S.No	Topology	Diode Clamped	Flying Capacitor	Cascaded H-Bridge
1.	Power semi conductor Switches	2(m-1)	2(m-1)	2(m-1)
2.	Clamping diodes per phase	(m-1) (m-2)	0	0
3.	DC bus capacitors	(m-1)	(m-1)	(m-1)/2
4.	Balancing capacitors per phase	0	(m-1) (m-2)/2	0
5.	Voltage un balancing	Average	High	very small

3. Modified Cascaded Five-Level Inverter

In modified cascaded five-level inverter, an auxiliary circuit is added in the simple H-bridge inverter. The output voltage of simple H-bridge inverter is the three-level voltage waveform, and to make it a five-level waveform, the auxiliary circuit is

Connected , which contains two back-to-back IGBT switches in series with the diodes. Figure 2 shows a single-phase modified cascaded five-level inverter. For +Vdc/2, switches S4 and S6 are on, for +Vdc, switches S1 and S4 are on, for –Vdc/2, switches S2 and S3 are on, for –Vdc, switches S2 and S5 are on, and for zero, either switches S4, S1 or switches S2, S4 is conduct shows in Table 2. Therefore, five-level inverter output voltage is obtained. Multicarrier sinusoidal PWM law has been adopted to generate the gating pulses for modified cascaded five-level inverter.

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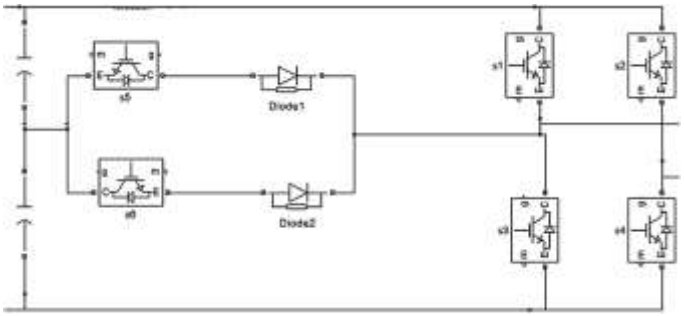


Fig. 2 Single-phase modified cascaded five-level inverter

Table 2: Inverter Output Voltage During S1-S5 switch On and Off

ON SWITCHES	V_a	V_b	$V_{ab}=V_0$
S4,S1	V_{dc}	0	$+V_{dc}$
S4,S6	$V_{dc}/2$	0	$+V_{dc}/2$
S4,S3	0	0	0
S2,S1	$V_{dc}/2$	$V_{dc}/2$	0
S2,S5	0	V_{dc}	$-V_{dc}$
S2,S3	0	$V_{dc}/2$	$-V_{dc}/2$

4. Pulse Width Modulation

Pulse-width modulation (PWM) of a signal or power source involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load .There are many forms of modulation used for communicating information. When a high frequency signal has amplitude varied in response to a lower frequency signal we have AM (amplitude modulation) When the signal frequency is varied in response to the modulating signal we have FM (frequency modulation.). These signals are used for radio modulation because the high frequency carrier signal is needs for efficient radiation of the signal. When communication by pulses was introduced, the amplitude, frequency and pulse width become possible modulation options. In many power electronic converters where the output voltage can be one of two values the only option is modulation of average conduction time.

There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate pulse width modulation (PWM) control within the inverters. The commonly used techniques are:

I. Single Pulse Width Modulation
II. Multiple Pulse Width Modulation
III. Sinusoidal Pulse Width Modulation
IV. Trapezoidal Pulse Width Modulation
V. Stair case Pulse Width Modulation

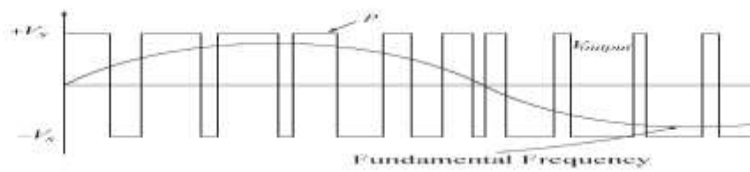
In PWM inverters, forced commutation is essential. The PWM techniques listed above differ from each other in the harmonic content in their respective output voltages. Thus, choice of a particular PWM technique depends upon the permissible harmonic content in the inverter output voltage. Industrial applications PWM inverter is supplied from a diode bridge rectifier and an LC filter. The inverter topology remains the same for a single phase inverter and for a three phase inverter. But now the devices are now switched ON and OFF several times within each half cycle to control the output voltage which has low harmonic content [11-14].

5. Sinusoidal Pulse Width Modulations

The width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency Fc. The frequency of reference signal Fr, determines the inverter output frequency and its peak amplitude Ar, controls the modulation index M, and rms output voltage Vo. The number of pulses per half cycle depends on carrier frequency.

6. Sinusoidal PWM Law

A fundamental period consists of p pulses whose widths vary sinusoidally throughout the cycle to give the fundamental component of frequency. The basis of equivalence between the desired sinusoid and the actual pulsed waveform is taken to be volt–seconds, i.e., As1 = Ap1 and As2 = Ap2.



Sinusoidal PWM Signal

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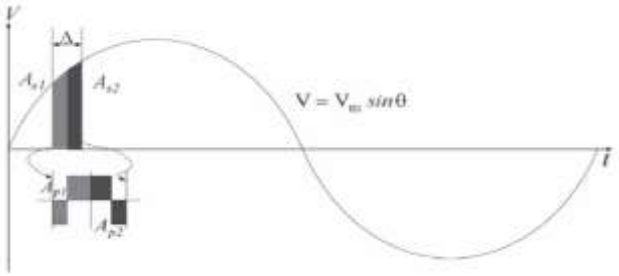
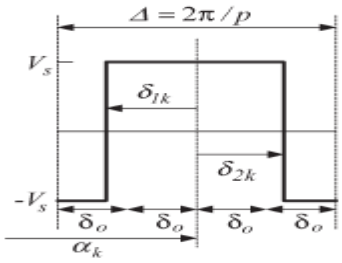


Basis of Equivalence for Sinusoidal PWM: Volt-Seconds



Characterization of Pulse

The switching period Δ and the frequency modulation ratio p are, respectively, given by

$\Delta = 2\pi/p$ ……. (3.2.1)

$p = fs/f1$ ……. (3.2.2)

where fs is the switching frequency and f1 is the fundamental frequency. The quarter period of pulse δ0 is given as

$\delta 0 = \Delta/4$. …… (3.2.3)

Ak is the position from the origin of the fundamental period of the midpoint of the period Δ. The angles δ1k and δ2k are the modulating angles which vary throughout the cycle, and it is to calculate these angles that a modulation law must be derived. Consider first the average voltages V 1k and V 2k during the two halves of the modulating pulse

$V1k=(Vs)\{\delta 1k-(2\delta 0-\delta 1k)\}/2\delta 0$ …… (3.2.4)

$\therefore V\ 1k = (Vs)\ (\delta 1k - \delta 0)/\delta 0 = (Vs)\beta 1k$ …. (3.2.5) Where, $\beta 1k = (\delta 1k - \delta 0)/\delta 0$ and, similarly

$V2k = (Vs)\beta 2k$ ……... (3.2.6)

Where, $\beta 2k = (\delta 2k - \delta 0)/\delta 0$.

The volt–second As1 is the half-pulse width of the sine wave and is given according to Fig. 8 by

$As1=$integral $(Vm\sin\theta d\theta)$ from αk to $\alpha k-2\delta 0$ …… (3.2.7)

$=2Vm \sin \delta 0 \sin (\alpha k - \delta 0)$.

However, $\sin \delta 0 \rightarrow \delta 0$ when δ0 is small

$\therefore As1=2\delta 0 Vm\sin(\alpha k-\delta 0)$ …. (3.2.8)

similarly, $As2=2\delta 0 Vm\sin(\alpha k+\delta 0)$ …… (3.2.9)

For the corresponding volt–second Ap1, in the PWM waveform, $Ap1 = 2\delta 0 V\ 1k$

$\therefore Ap1 = 2\delta 0 \beta 1k(Vs)$ …. (3.2.10) and, similarly, $Ap2 = 2\delta 0 \beta 2k(Vs)$. …. (3.2.11)

For equivalence of volt–seconds from which the modulation law can be derived, we require that

$As1 = Ap1$ …… (3.2.12)

$As2 = Ap2$ …… (3.2.13)

From above relations

$\beta 1k = M \sin (\alpha k - \delta 0)$ …… (3.2.14) and similarly,

$\beta 2k = M \sin (\alpha k + \delta 0)$ …… (3.2.15)

where M is the "modulation index" and

$M = Vm/Vs$. …… (3.2.16) Here β1k and β2k are the functions of sinusoidal wave hence it can be stated that the output PWM wave is nearly to the sinusoidal variations in its magnitude .

7. Adopted Pulse Width Modulation

Figure 3 shows the pulse width modulation for generating gate pulses of single phase MCFLI. To obtain the five-level PWM, reference sine wave is compared with two triangular carrier waves of high frequency (about 1.6–2 kHz). First, Vref is compared with the carrier 1 as Vref [Vc1 up to Φ1. After Φ2, Vref is compared with Vc2 and similar outputs received. If modulating index is (Ma) > 0.5, the output will be a five level. Modulating index is Ma = Am/2Ac, where Am is amplitude of modulating (reference) signal and Ac is the amplitude of carrier signal.

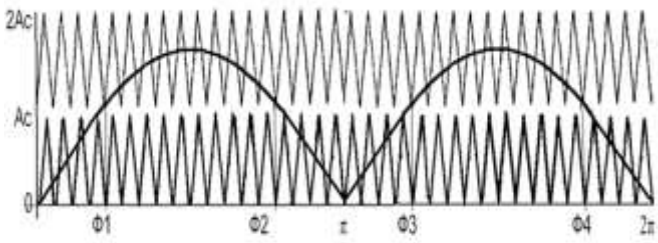


Fig. 3 Pulse width modulation for generating the gate pulses

8. Simulation Results

Figure 4 shows the modified cascaded five-level inverter for a single phase. Here, only six controlled switches are used to get five levels which reduced the complexity of the circuit and the total harmonic distortion as compared to conventional inverter.

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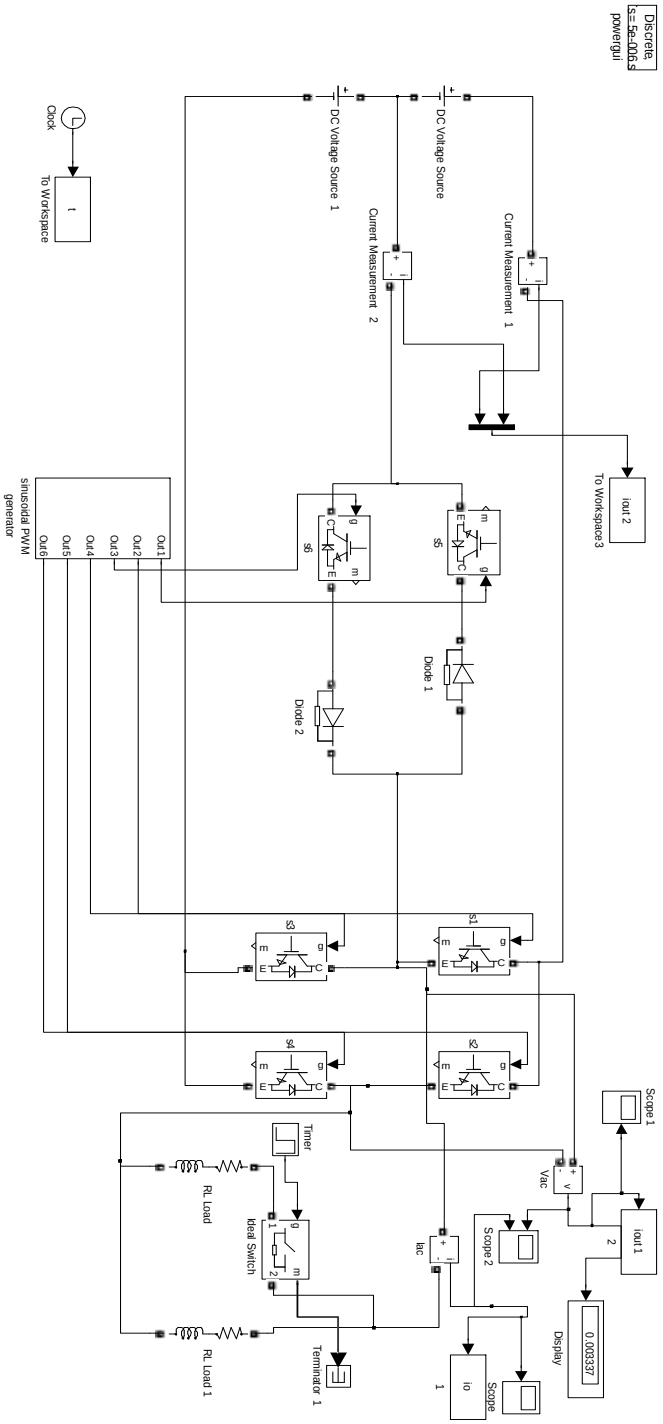

Fig. 4 MATLAB/Simulink model for modified cascaded five-level inverter

Figures 5, 6, 7, 8, 9 and 10 show the phase voltage, line voltage, current and THD of a modified cascaded five-level inverter. We can say that the distortion in five-level inverter voltage is less.

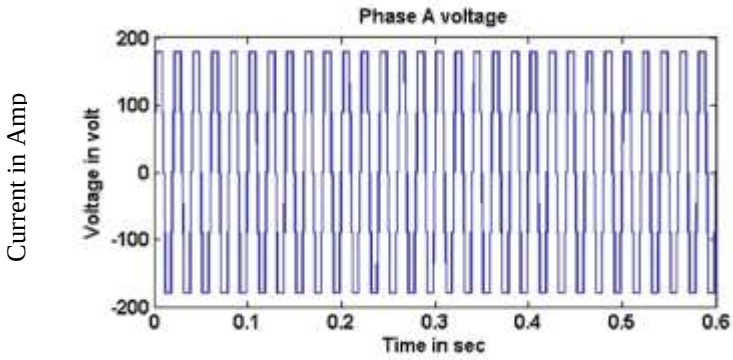

Fig. 5 Phase voltage of a modified cascaded five-level inverter

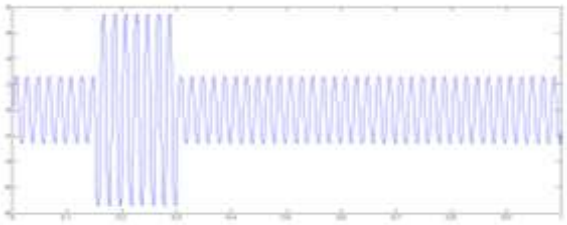

Fig. 6 Line voltage of a modified cascaded five-level inverter

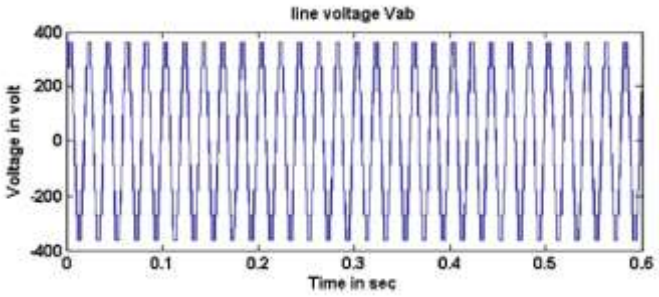

Fig. 7 Load current of a modified cascaded five-level inverter

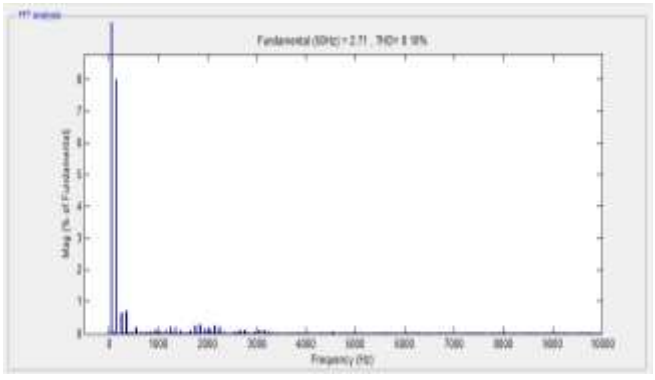

Fig. 8 Harmonic spectrum of load current of modified cascaded five-level inverter

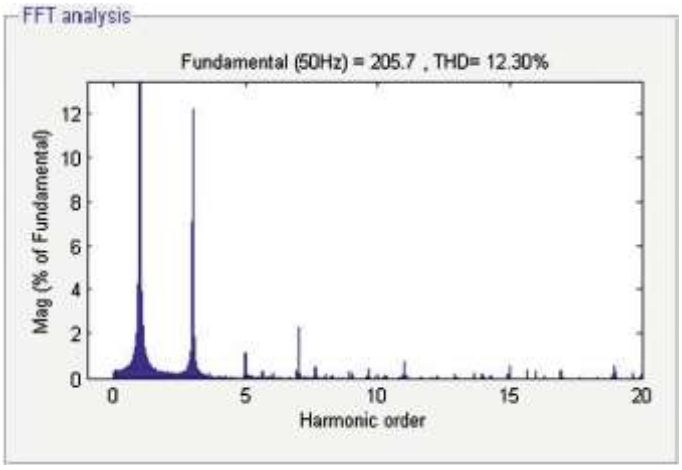

Fig. 9 Harmonic spectrum of phase voltage of modified cascaded five-level inverter

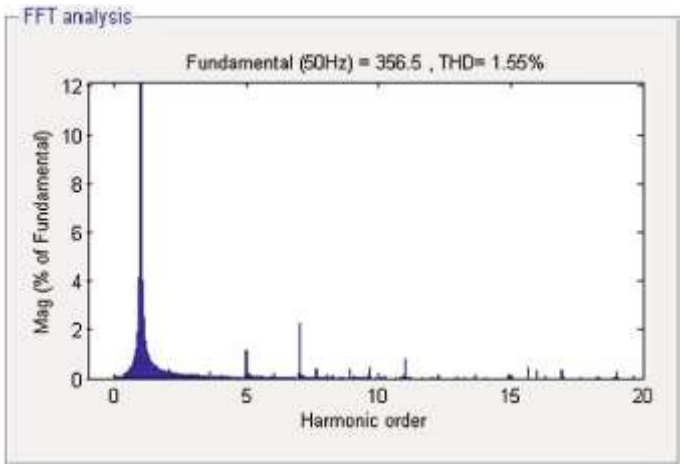

Fig. 10 Harmonic spectrum of line voltage

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