

# A Feasible Approach to Design a Cmos Domino Circuit at Low Power VLSI Application Design

Pallavi Sharma<sup>1</sup>, Dr Subodh Wariya<sup>2</sup>

<sup>1</sup>Electronics Engineering Department, Institute of Engineering and Technology,  
Uttar Pradesh Technical University Road,  
Lucknow-226021, U.P India  
[niec1989.ec@email.com](mailto:niec1989.ec@email.com)

<sup>2</sup>Electronics Engineering Department, Institute of Engineering and Technology,  
Uttar Pradesh Technical University Road,  
Lucknow-226021, U.P India  
[swariya@ietlucknow.edu](mailto:swariya@ietlucknow.edu)

**Abstract:** Dynamic logic style is used in high performance circuit design because of its fast speed and less transistors requirement as compared to CMOS logic style. But it is not widely accepted for all types of circuit implementations due to its less noise tolerance and charge sharing problems. A small noise at the input of the dynamic logic can change the desired output. Domino logic uses one static CMOS inverter at the output of dynamic node which is more noise immune and consuming very less power as compared to other proposed circuit. In this paper we have proposed a novel circuit for domino logic which has less area and has less power-delay product (PDP) as compared to previous reported articles. Low PDP is achieved by using semi-dynamic logic buffer and also reducing leakage current when PDN is not conducting. Then comparison analysis has been carried out by simulating the circuits in 90nm CMOS process technology from TSMC using Tanner EDA 14.11.

Keywords: Dynamic logic, Dynamic Node, High speed, Diode Footed Domino, Noise Tolerance, Propagation delay, Power Consumption, Robustness, Domino CMOS logic.

## 1. Introduction

The rapid advancement in VLSI circuit is due to increased use of portable and wireless systems with low power budgets and microprocessors with higher speed. To achieve this, the size of transistors and supply voltages are scaled down along with technology. Due to larger number of devices per chip the interconnection density increases. The along with high clock frequency increases capacitive coupling of the circuit. Therefore, noise pulses known as crosstalk are generated leading to logic failure and delay of the circuit. Again, when supply voltage is scaled, threshold voltage of the device needs to be scaled to preserve the circuit performance, which in turn leads to increase in the leakage current of the device. Due to high speed and low device count especially compared to complementary CMOS, dynamic-logic circuits are used in a wide variety of applications including microprocessors, digital signal processors and dynamic memory. Dynamic circuit contains a pulldown network (PDN) which realizes the desired logic function.

1. At the evaluation period when all the inputs are at logic 0, the dynamic node should be at logic 1. But the NMOS pull-down leaks the charge stored in the capacitance at the dynamic node due to the sub threshold leakage. This is again compensated by the PMOS keeper, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at ant gate input, the keeper may not be able to restore the voltage level of the dynamic node. The sub threshold leakage current is exponentially dependent upon VGS. So in the presence of noise impulse the gate voltage increases, which leads to increase in VGS and the dynamic node gets wrongly discharged.

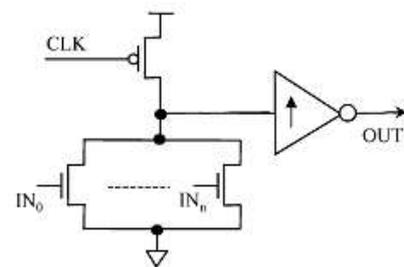


Figure 1. Domino or Gate

## 2. Basic Domino Theory

Figure 1 is an example of footless domino gate. During the precharge phase when the clock is LOW, the pre-charging gets ON and the dynamic node is connected to the VDD and gets precharge to VDD. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic

### 3. Background and related work

#### 3.1 Standard Domino Or Gate

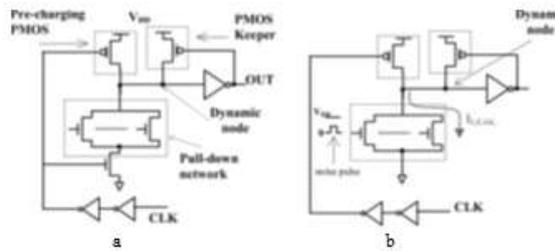


Figure 2. Standard domino OR gate

a. Footed scheme

b. Footless scheme

To compensate the leakage current at the dynamic node transistor called keeper transistor is used. Keeper transistor prevents the charge loss and keeps the dynamic node at strong high when PDN is OFF. In the first domino proposal [3] the gate of the keeper transistor is tied to ground, therefore the keeper is always on. If at the beginning of evaluation the pull-down network (PDN) turns on, the dynamic node tends to discharge through the PDN. However, the keeper is injecting charge to the dynamic node as it is always on. This is called contention. Furthermore, a potential DC power consumption problem is generated. To alleviate the potential DC power consumption problem a feedback keeper was proposed in Figure. 2a.

#### 3.2 Previous works showing Or Gate

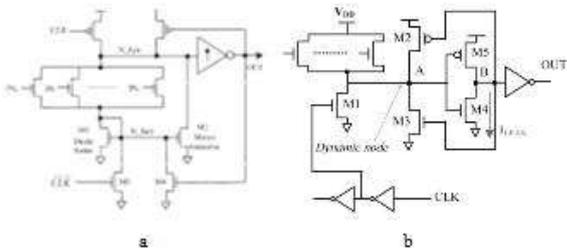


Figure 3. Previous works showing OR gate

a. Diode footed Domino [6]

b. Domino circuit in scheme [7]

In [6], this Diode-Footed domino an NMOS transistor is there in a diode configuration i.e. gate and drain terminals connected together in series with the evaluation network, as shown in Figure 3a. A diode connected transistor is exploited in this design in which the leakage flowing through the PDN in the evaluation phase causes the voltage drop across the diode transistor. Which makes the  $V_{GS}$  negative and leakage reduces. The performance degradation can be compromised by the mirror network. In [7] the circuit based on a pull up network constitutes only the NMOS transistors as depicted in Figure 3b. This style doesn't have precharge PMOS transistors. When the clock is low i.e. at the precharge stage M1 is switched on the dynamic node is pre-charged to 0 V. When clock is high i.e. at evaluation phase M1 is off and the pull up network conditionally can charge the dynamic node.

#### 3.3 Previously proposed Domino Circuit

A previously proposed novel domino circuit scheme is shown in Figure 4. Transistor M4 is used as stacking transistor. Due to voltage drop across M4, gate-to-source voltage of the NMOS transistor in the PDN decreases (stacking effect). The purpose of M5 in proposed scheme causes the stacking effect and makes gate-to-source voltage of M3 smaller (M3 less conducting). Hence circuit becomes more noise robust and less leakage power. But for performance degrades because of

stacking effect in mirror current path. This can be increased widening the M2 (high W/L) to make it more conducting. The use of extra transistor has increased the area which has caused a problem of more routing issues and delay of output due to increased path and more links to be traversed to reach the destination port

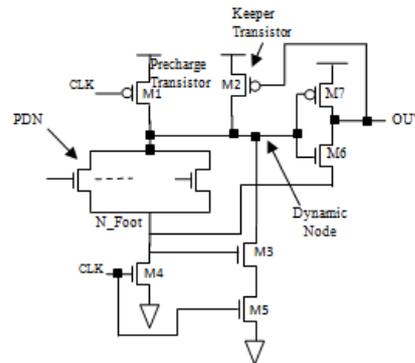


Figure 4. Previously Proposed Circuit

### 4. Proposed work

#### 4.1 Circuit analysis

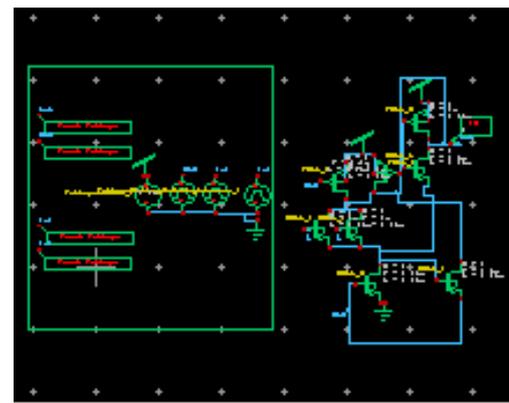


Figure 5: Proposed Scheme

The above proposed circuit has reduced no. of transistor the M5 used in the previously designed one has been eliminated and reduced area is major advantage of this proposed one Here below the pulldown network two transistor M3 and M4 is used. When input is applied the output remains at high only if no high input is applied to the pulldown network the additional transistors M3 and M4 is being provided to pull down the dynamic node low if pulldown network is high thus dynamic node is at once pulled down through M3, 4 without any delay without the attacking of transistors the other arrangements are usual with a pmos being provided to compensate for the leakage.

As keeper transistor prevents charge loss in the similar way M3 and M4 transistors prevents delay of output going low as whenever a voltage drop occurs across M4 due to presence of noise signal then M3 as it can be seen is connected to drain of M4 and hence gate of M3 has voltage drop and whatever voltage is there at drain of M3 which is at same potential as pulldown prevents voltage or the dynamic node to get discharged abruptly

#### 4.2 Noise performance

Noise is any unwanted interference in the circuit which produces erroneous output. The possibility to reduce the noise entirely depends on the presence of extra inter connection links which depends on no. of transistors used extra devices means extra routing paths and delays of input signal to reach the output node. In the proposed circuit it can be easily seen that by eliminating the extra transistor reduced and unnecessary time delay for charge up time get reduced. When the PDN is OFF and the N\_Dyn is at high voltage and the N\_Foot is at low voltage. The high level of dynamic node makes the gate of the NMOS M6 of the buffer VDD and the low level of N\_Foot makes the source of the M6 to 0. It can be easily verified that if the NMOS transistor of the buffer can always be turned off, the pulses propagating to the output can be avoided or the time required to charge up the dynamic node will get reduced.

### 4.3 Power Analysis

The previously proposed structure uses the semi-dynamic buffer structure. The power consumption of the logic circuit in conventional circuit is given as follows  $5.97E-8$ .

In which it mainly depends on  $T_{on}$  which is the time when input logic is on,  $T_{off}$  which is the time when input logic is off and the probability of the state that the input logic change in a unit time the dynamic capacitor in on state,  $V_{noise}$  which is the pulse at the dynamic node which can be due to undue impulses.

The power analysis of the proposed circuit offers low power dissipation and the performance is better analyzed when we decrease or increase the W/L ratio by 1 to 1/10

## 5. Simulation Results

The circuits were simulated with using Tanner EDA tool using TSMC 90 nm technology using 1 V. The circuit was being compared with the OR gate previous techniques. The OR gate was implemented because it is a typical example of wide pull-down network. The proposed circuit was being implemented for OR gate and being compared with the OR gate of other reference circuits it was found that the proposed circuit performs better than the previous proposed circuits. It can be seen from the table that the proposed circuit is having less number of transistor and thus less no. of transistor means less area and less area caters more space allocation and moreover less power dissipation. The comparison Table 1 of various modified circuit gives an insight into the improvement scope. and W, L ratio variation direct relation with power dissipation and as power dissipation reduces the Figure of Merit of any device will automatically get increased another Table 2 shows the PDP of various circuit.

The PDP of the revised circuit is  $98.534E-17$  Watt-sec on an average. The average delay of the proposed circuit is  $16.50E-9$  and average power dissipated is  $5.97E-8$ .

**Table 1.** Comparison table

Circuit type	Domino or gate diode footed[6]	Previous Proposed scheme[7]	Existing	Proposed
No. of Extra Transistor	12	11	9	8
Use of Inverting Clock	Yes	Yes	No	No

**Table2.**Power delay Product Comparison of Proposed circuit with the previous work

	Domino or gate diode footed[6]	Previous Proposed Scheme [7]	Existing	Proposed
1	5.6E-14	5.8E-17	2.99E-17	26.02E-17
0.9	4.09E-14	9.09E-17	2.67E-17	2.01E-17
0.8	2.90E-14	1.57E-17	26.97E-18	1.30E-17
0.7	1.87E-14	1.48E-17	24.90E-18	14.31E-18
0.6	11.09E-14	1.65E-17	19.80E-18	23.03E-18
0.5	5.53E-14	4.06E-17	19.61E-18	22.29E-18

The major table no. 3 drawn below showing comparison of various circuits with the recent proposed work gives a detailed account of major contribution of the recent work. The earlier schemes used inverting clock which the recent work does not use also the recent research emphasizes on the reduced use of transistors.

The research is mainly focused on reduced propagation delay and power dissipation. The lesser use of transistor is an added advantage of the work. The performance of the proposed circuit was checked by changing the size of the extra transistors used for increasing the circuit performance.

The size of M3 and M4 were decreased below 1 up to 0.1 and increased from 1 to 10. With this variation the outputs were calculated and graphs were plotted. The circuit gives better performance when W/L ratio is closed to 1. The PDP reduction of the recent proposed scheme is far better than the previous work being done. The various values of PDP at different voltage values may increase or decrease but overall the average value is less by a marginal difference viable enough for comparison purposes.

**Table 3:** Power and Delay comparison.

Supply Voltage in Volt	Parameters	Basic Domino Footless and Keeper less	Basic Domino Footless and with Keeper	Basic Domino Footed and with keeper	Scheme on Paper[6]	Scheme on Paper[7]	Previously Proposed	Modified
1	Delay	1.57E-11	2.40E-11	4.109E-8	1.23E-9	1.04E-9	2.1180e-009	1.1820e-009
	Power	3.33E-5	3.32E-5	5.6E-6	4.58E-5	5.6E-8	1.4200e-008	2.0150e-008
0.9	Delay	1.78E-11	2.69E-11	4.10E-8	1.28E-9	1.05E-9	2.2641e-009	1.2773e-009
	Power	2.39E-5	2.39E-5	9.6E-6	3.20E-5	8.58E-8	1.1793e-008	1.5875e-008
0.8	Delay	2.08E-11	3.13E-11	4.111E-8	1.32E-9	1.06E-9	2.8192e-009	1.0609e-009
	Power	1.62E-5	1.62E-5	2.8E-5	2.20E-5	1.49E-8	9.6034e-009	1.2357e-008
0.7	Delay	2.52E-11	3.82E-11	4.00E-8	1.35E-9	1.09E-9	3.2629e-009	1.5187e-009
	Power	1.01E-5	1.01E-5	1.14E-5	1.39E-5	1.39E-8	7.6484e-009	9.4275e-009
0.6	Delay	3.29E-11	5.04E-11	4.01E-8	1.42E-9	1.15E-9	3.3856e-009	3.3006e-009
	Power	5.56E-6	5.56E-5	1.4E-5	7.81E-5	1.44E-8	5.8647e-009	6.9825e-009
0.5	Delay	4.90E-11	7.73E-11	4.16E-8	1.58E-9	1.31E-9	4.5282e-009	4.4835e-009
	Power	2.44E-6	2.46E-5	1.4E-5	3.50E-5	3.1E-8	4.3423e-009	4.9772e-009

## 6. Graphs

### 6.1 Graphical representation of the circuit power and delay.

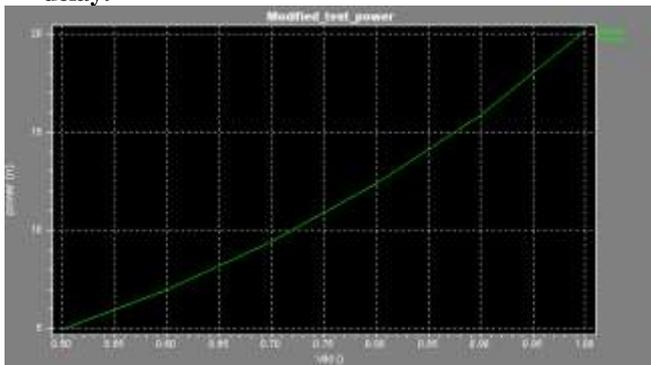


Figure6. a) Power Graph

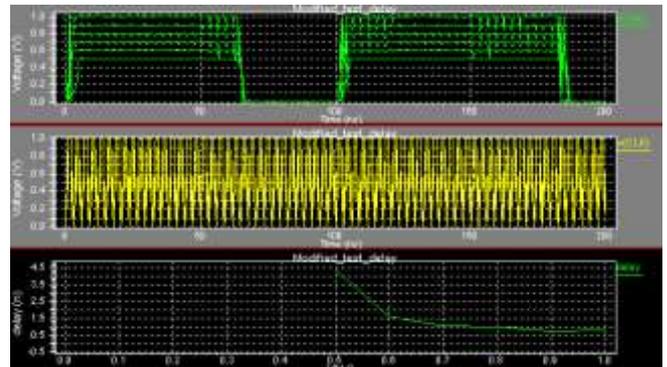
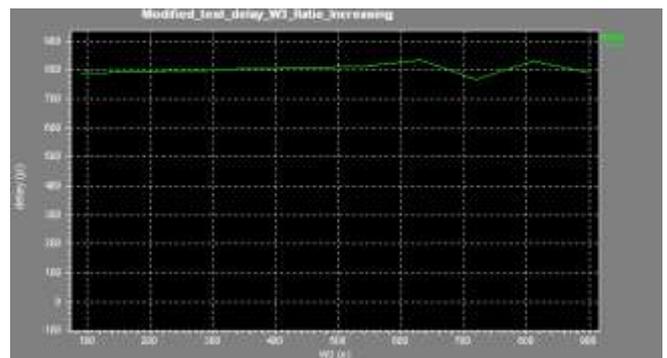
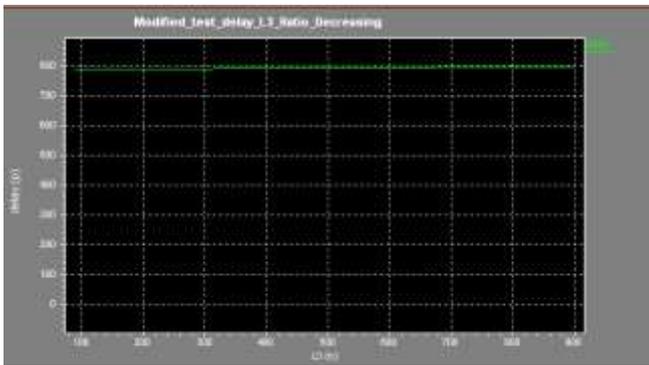


Figure6 b) Delay Graph

### 6.2 Graphs showing variation of W/L ratio on the circuit.

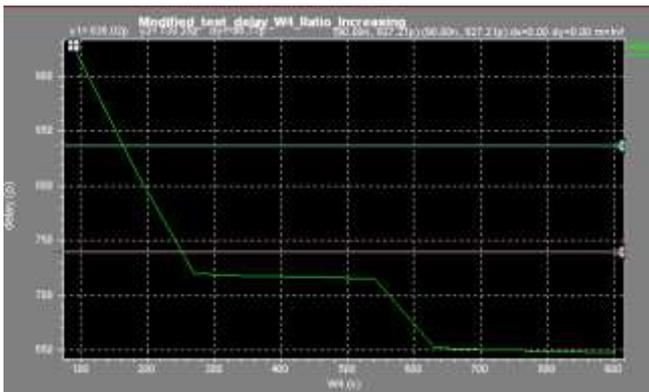


a) Graph of W3 ratio increasing

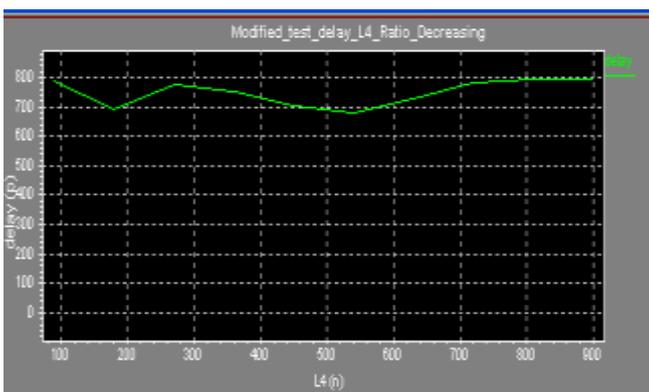


b) Graph of L3 ratio decreasing

**Figure 7.** W/L variation of M3



a) Graph of W4 ratio increasing



b) Graph of L3 ratio decreasing

**Figure 8.** W/L variation of M4

## 7) Conclusion and future scope

In this paper, we have proposed a high-speed and low power domino logic circuit, which also have noise-tolerance in the output node as there are lesser nodes to travel for the signal and because of which any circuit will show less noisy level. The simulation was done with Tanner 90 nm TSMC technology and 1 V CMOS process and edited in Wedit. The results have shown that the proposed scheme can work with very high speed and also consuming low power, which reduces the area of the circuit. Proposed circuit also shows noise efficiency because the noise of the output buffer dramatically improved as compared to previous work. Also the circuit is flexible for wide variety of dynamic logic styles and adequate for large gates incorporation.

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## Authors Profile



**Pallavi Sharma** has done B-tech from Northern India Engineering College Affiliated to Uttar Pradesh Technical University in 2011. She is doing M-tech from Institute Of Engineering and Technology Lucknow in Microelectronics she is keen to work in the field of low power Microelectronics having low power dissipation and reduced area.



**Dr. Subodh Wairya** received B. Tech (1993), M.Tech and PhD (2012) from HBTI, Kanpur, Jadavpur University, Kolkata and MNNIT Allahabad, India, respectively. His PhD research work was oriented towards PERFORMANCE EVALUATION

OF HIGH SPEED LOW POWER CMOS FULL ADDER CIRCUITS FOR LOW VOLTAGE VLSI DESIGN. Currently, he is an Associate Professor at IET, Lucknow (from 6 May 1996- Present). He has also served as Scientist "B" Adhoc (One Year) at DRDO Lucknow during January, 1995-January, 1996 and Graduate Engineer under Consultancy Project at HAL, Lucknow during From January, 1994- January, 1995 (one year). Also he is one of the authors of a book titled "A Simplified Approach to Telecommunication and Electronic Switching Systems" by C.B.L. Srivastava, Neelam Srivastava & Subodh Wairya Published by Dhanpat Rai and Company.