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FPGA Implementation of Binary Coded Decimal Digit Adder and Multiplier

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I. INTRODUCTION

Arithmetic has gained high impact on the overall performance of today's financial and commercial applications. Decimal additions and multiplication are the main decimal operations used in any decimal arithmetic algorithm. Decimal digit adders and decimal digit multipliers are usually the building blocks for higher order decimal adders and multipliers. FPGAs provide an efficient hardware platform that can be employed for accelerating decimal algorithms.

Although binary calculations are the dominant in most machines, they are not suitable for commercial, banking, and business applications due to the unacceptable inexact decimal to-binary conversion errors they produce. In a real example shows the extreme effect of these wrong approximations, where it stated that if a communication company approximates a 5% sales tax on an item , the yearly loss is over than a $5 million.

Further, the survey in showed that 55% of the numeric data columns, used by 51 major organization's databases, were decimal data types and 43.7% were integer types which could have been stored as decimals. In spite of this, currently, decimal floating-point arithmetic is not supported by any microprocessors. Decimal floating-point coprocessor could be included in the machines that handle these calculations to speed up these applications.

In order to convoy the growing evolution of the decimal arithmetic, efficient decimal algorithms have to be investigated. Decimal digit adders and decimal digit multipliers are key components of any decimal hardware to support decimal arithmetic applications. Therefore, this work focuses on delivering efficient BCD digit units to be used in high performance decimal hardware accelerators.

Two main contributions of this work can be highlighted: proposing two new BCD digit adders and proposing one new BCD digit multiplier. These designs are described and simulated using VHDL hardware description language. They are all implemented on an FPGA an compared with existing designers.

II. LITERATURE REVIEW

The rigorous review of related work and published literature, it is observed that many research From tars have The addition of two n-digit BCD numbers follows the same procedure. After binary addition of any decimal pair, the result is checked for correctness. Then, the correct decimal carry output is passed to the next more significant digit pair, to be added with the two decimal digits located in the same position. The conditional addition of 6 in each decimal digit position adder architecture for each decimal digit. The long carry chain for such BCD adder slows down the addition operation. Therefore, to improve the BCD adders speed, designers have proposed several enhancements to the basic BCD addition algorithm .Direct decimal addition , decimal speculative addition and conditional speculative decimal addition, are examples of such refinements.

1. REKHA K. JAMES and SHAHANA T. K, from Cochin University of Science and Technology Kochi, Kerala, India are work on the Decimal Multiplication using compact BCD Multiplier. In 2008 IEEE International Conference on Electronic Design

Decimal multiplication is an integral part of financial, commercial and internet-based computations. The basic building block of a decimal multiplier is a single digit multiplier. It accepts two Binary Coded Decimal (BCD) inputs and gives a product in the range [0, 81] represented by two BCD digits. A novel design for single digit decimal multiplication that reduces the critical path delay and area is proposed in this research. Out of the possible 256 combinations for the 8-bit input, only hundred combinations are valid BCD inputs. In the hundred valid combinations only four combinations require 4 x 4 multiplication 64, combinations need 3 x3 multiplication, and the remaining 32 combinations use either3 x4 or4 x3 multiplication. The proposed design makes use of this property. This design leads to more regular VLSI implementation, and does not require special registers for storing easy multiples.

In this shows the a novel design for single digit decimal multiplication to reduce the critical path delay and area, which allows for a fast multiplier design. The accumulation of partial products generated using single digit multipliers is done by an array of multi-operand BCD adders for an (n-digit n-digit) multiplication. This is a fully parallel multiplier utilizing only combinational logic, and can be extended for floating point multiplication of decimal digits.

Advantage is demonstrated that this design gains a 7% savings in the area and 16% savings in delay compared to the existing design of . This design leads to more regular VLSI implementation, and does not require special registers for storing easy multiples of these .

2. Alvaro Vazquez, Member, IEEE, Elisardo Antelo he is worked on the Improved Design of High-Performance Parallel Decimal Multipliers in the IEEE TRANSACTIONS ON COMPUTERS, VOL. 59, NO. 5, MAY 2010

The new generation of high-performance decimal floating-point units (DFUs) is demanding efficient implementations of parallel decimal multipliers, He describe the architectures of two parallel decimal have presented several

techniques to implement decimal parallel multiplication in hardware. He propose two different SD encodings for the multiplier that lead to fast parallel and simple generation of partial products He have developed a decimal carry-save algorithm based on unconventional (4221) and (5211) decimal encodings for partial product reduction. It makes possible the construction of p:2 decimal CSA trees that outperform the area and delay figures of existing proposals. He have proposed architectures for decimal SD radix-10 and SD radix-5 parallel multiplication. The area and delay figures from a comparative study including conventional binary parallel multipliers and other representative decimal proposals show that our decimal SD radix-10 multiplier is an interesting option for high performance with moderate area.

3. Álvaro Vázquez are work on Multi-operand Decimal Adder Trees for FPGAs is publish in INRIA version1 - 14 Oct 2010

The research and development of hardware designs for decimal arithmetic is currently going under an intense activity. For most part, the methods proposed to implement fixed and floating point operations are intended for ASIC designs. Thus, a direct mapping or adaptation of these techniques into a FPGA could be far from an optimal solution. To improve the efficiency of Virtex-5/6 implementations we have developed a new algorithm for BCD carry-propagate addition. Combinational and pipelined versions of the BCD multi-operand adder were synthesized in a Virtex-6 speed grade-3 device and the results compared with a binary carry-ripple adder tree and a BCD multi-operand adder tree build of BCD carry-chain adders .He show that the proposed design is a very competitive option for high-performance low- low-latency implementations of BCD multiplication on Virtex-5/6 FPGAs at a moderate hardware cost.

4. L. Dadda work on A Parallel-Serial Decimal Multiplier Architecture is published in 2012 IEEE 15th International Conference on Computational Science and Engineering

Derived from a parallel multiplier, a parallel-serial decimal multiplier is proposed in which the multiplicand is assumed in parallel whereas the multiplier is in digit-serial form. A scheme for a parallel-serial decimal multiplier is presented, using BCD digits. The multiplicand is assumed in parallel, the multiplier in digit-serial form. The values of the Digit Products in the successive columns of the product array are added in binary and converted in decimal. Their decimal alignment generates a set of three or four serial decimal numbers whose sum is the product. The product digits are obtained via a serial multioperand adder. The evaluation of the Columns needs the largest part of the total area. Its scheme is *naturally* pipelined, offering a high processing speed. The case of multipliers in which two consecutive multiplications are overlapped in time has also been treated.
In trying to identify new efficient and less resource demanding solutions, Hearer also investigating a new version of the multiplier, which will try to take advantages by the resources available on the FPGAs.

5. Osama D. Al-Khaleel i FPGA implementation of Binary Coded Decimal Digit Adders and Multipliers published a paper in 2012 IEEE

Decimal arithmetic has gained high impact on the overall performance of today's financial and commercial applications. Decimal additions and multiplication are the main decimal operations used in any decimal arithmetic algorithm. Decimal digit adders and decimal digit multipliers are usually the building blocks for higher order decimal adders and multipliers. FPGAs provide an efficient hardware platform that can be employed for accelerating decimal algorithms. In this paper, different designs for two decimal digit adders and one decimal digit multiplier are proposed.

In it two new BCD digit adders and one new BCD digit multiplier are designed for the purpose of speeding up decimal arithmetic applications over FPGAs. Each design is described, verified and tested for a correct functionality using VHDL coding and simulation. The different designs are implemented using Xilinx ISE10.1 Up to these all worked up to simulations we are extend it up to the performance on the board.

II. Proposed Work

Binary coded decimal digit multiplier is a fundamental cell in the BCD multiplication operation. It multiplies two BCD digits to produce a two BCD digits product output. We have discussed many BCD digit multiplier approaches In this section, we introduce a new BCD digit multiplier architecture also that manipulates directly with BCD representation form.

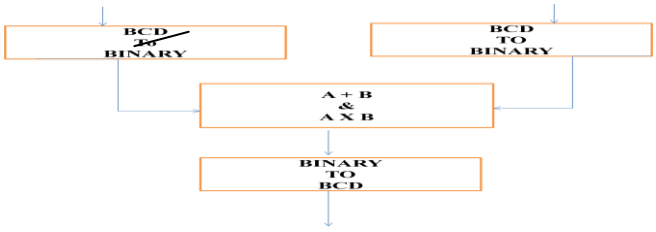


Fig. Basic block dig

1. Proposed BCD Digit Adder:

The main problem in decimal addition, that increases the delay, is the need for correction if the result exceeds the permitted BCD range (decimal number 9). This correction actually adds the binary number (0110)2 to the result. One contribution in this work is the design of new high-speed area-optimized correction-free BCD digit adders that can be employed in different decimal applications.

2. Proposed BCD Digit Multiplier

Binary coded decimal digit multiplier is a fundamental cell in the BCD multiplication operation. It multiplies two BCD digits to produce a two BCD digits product output. We have discussed many BCD digit multiplier approaches. a new BCD digit multiplier architecture that manipulates directly with BCD representation form.

III. Objective

1. Study the different architecture of BCD Adder &Multiplier
2. Design the efficient using VHDL
3. Measure the performance of design in terms of resource utilization &timing parameter.
4. Optimize the delay of design

IV. Software Tools

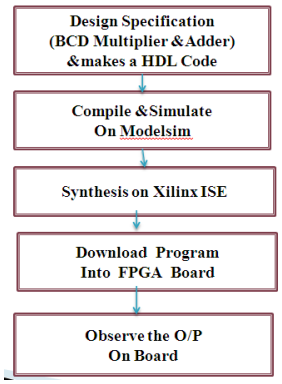
1. Modelsim

ModelSim is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed language designs.

2. Xilinx ISE

Xilinx Integrated Software Environment (ISE) is a software tool developed by Xilinx corporation for the synthesis and analysis of Hardware Descriptive Language (HDL) designs. It enables the synthesis of designs, timing analysis , Register Transfer Level (RTL) diagram examinations, simulation as per different environments as well as the configuration of the target device with the help of the programmer.

V. DESIGN PROJECT FLOW CHART



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