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A Grid Connected Three Phase PV Quasi-Z-Source Inverter with Double Frequency Ripple Suppression Control

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***Abstract*- In a Grid connected three-phase photovoltaic (PV) system, there is double-frequency power mismatch existed between the dc input and ac output. The double-frequency ripple (DFR) energy needs to be buffered by passive network. Otherwise, the ripple energy will flow into the input side and adversely affect the PV energy harvest. In a conventional PV system, electrolytic capacitors are usually used for this purpose due to their high capacitance. However, electrolytic capacitors are considered to be one of the most failure prone components in a PV inverter. In this project, a capacitance reduction control strategy is proposed to buffer the DFR energy in three-phase Z-source/quasi-Z-source inverter applications. Without using any extra hardware components, the proposed control strategy can significantly reduce the capacitance requirement and achieve low input voltage DFR. Consequently, highly reliable film capacitors can be used. The increased switching device voltage stress and power loss due to the proposed control strategy will also be discussed. The proposed system is simulated in MATLAB/Simulink platform.**

***Index Terms*-** DC-link voltage balance, Zero voltage switching, Renewable Energy (RE).

I. INTRODUCTION

The voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) have been considered for photovoltaic (PV) application in recent years [1]–[13]. These inverters feature single-stage buck–boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications [1]–[5]. The single phase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance [6]–[12]. In three-phase applications, the Z-source (ZS)/quasi-Z-source (qZS) network only needs to be designed to handle the high frequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present the proposed control strategy. A single-phase qZSI system is shown in Fig. 1. Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency. The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C1 which has higher voltage rating thanC2. The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected. Electrolytic

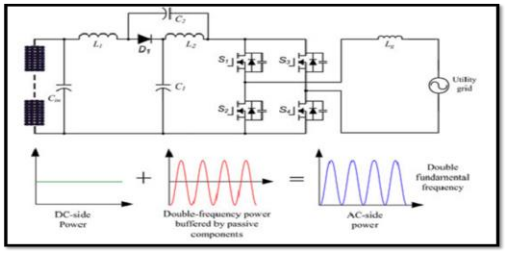

Fig. 1. Diagram of a single-phase qZSI-based PV system

capacitors contain a complex liquid chemical called electrolyte to achieve high capacitance and low series resistance. As the electrolytic capacitors age, the volume of liquid present decreases due to evaporation and diffusion. This process is accelerated with higher temperature, eventually leading to performance degradation over time [14]. Therefore, electrolytic capacitors are considered to be the weak component regarding to lifetime, especially under outdoor operation conditions. Accurate analytical models to calculate the DFR for qZSI have been developed in [8], [15], and [16] and the design guidelines for selecting the capacitance to limit the DFR are also provided. Nevertheless, the required capacitance is still large. In [17], two additional smoothing-power circuits are employed to reduce the DFR of dc-link voltage in ZSI. However, the added circuits increase the system cost and complexity. In [18], a low frequency harmonic elimination PWM technique is presented to minimize the DFR on Z-source capacitors. However, the method is used for application with constant voltage input source and DFR current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels. In some reported single-phase two-stage system which is composed of a dc–dc converter and H-bridge inverter, the dc link capacitance

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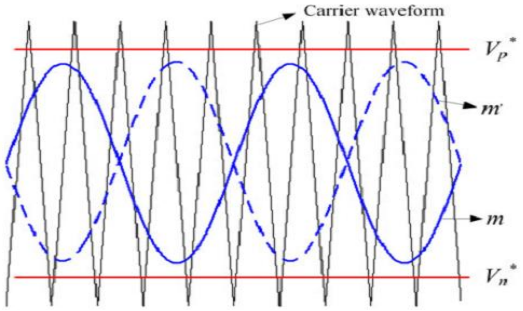
can be significantly reduced by using dedicated control [14]. However, the qZSI does not have the dc–dc stage, so the reported capacitance reduction methods cannot be applied in the qZSI. In this project, a new control strategy is proposed for ZSI/qZSI to mitigate the input DFR without using large capacitance, which enables us to use the highly reliable film capacitors. There is no extra hardware needed to implement the capacitance reduction. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. In order to apply the capacitance reduction method, it is necessary to study the impact of decreasing the capacitance on system design and performance.

II. OPERATION OF CONVERTER

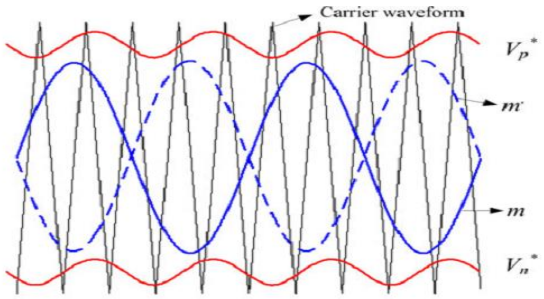
The basic principle of the proposed capacitance reduction method can be explained by

$$\Delta E = \frac{1}{2} C \left(v_{C\_\max}^2 - v_{C\_\min}^2 \right) \quad \text{.....1}$$

Where C is the capacitance, ΔE is the ripple energy that is stored in the capacitor, and v_{Cmax} and v_{Cmin} are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increase ΔE. One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor. Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input. In order to achieve this, a modified modulation strategy and an input DFR suppression controller are presented. In conventional single-phase qZSI, the modulation strategy is shown in Fig. 3.2(a). The two phase legs of the full bridge are modulated with 180° opposed reference waveforms, m and m' to generate three-level voltage output. Two straight lines v^*_p and v∗n are used to generate the shoot through duty ratio. When the triangular carrier is greater than v^*_p or the carrier is smaller than v∗n, all four switches S1−S4 turn on simultaneously for shoot-through. In the proposed control system, the shoot-through control lines v^*_p and v^*_n are modified to a line with double-frequency component as shown in Fig. 3.2(b). By doing so, the dc side and the qZS capacitor DFR can be decoupled. An input DFR



(a)



(b)

Fig. 2. Modulation strategy of (a) traditional method and (b) proposed method.

suppression controller is added in the control system to generate the double-frequency component in v^*_p and v^*_n.

Fig..3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, grid connected current controller, qZS capacitor voltage controller, and input DFR suppression controller. The MPPT controller provides the input voltage reference v^*_{IN}. The error between v^*_{IN} and v_{IN} is regulated by a PI controller and its output is the magnitude of the grid current reference. The grid current ig is regulated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency.

The qZS capacitor voltage is regulated by controlling dSH. The shoot through lines can be generated as v∗p =1−dSH and v∗n=−1+dSH. It is noted that v_{C2} is used for the capacitor voltage control. This is because v_{C2} signal will be used for the qZS network oscillation damping. The oscillation is mainly caused by the resonance among the C2 and inductors. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and v_{C2} information is required for the implementation. The v_{C2} voltage controller only regulates the average value ofvC2, which is V_{c2_ave}, due to the low-pass filter in the signal feedback with a cutoff frequency of 25 Hz. Therefore, the capacitor voltage controller has limited influence on double-frequency component and most DFR energy can be kept in qZS capacitors. The reference $V^*_{c2\_ave}$ is synthesized using the reference value of the average dc-link voltage, V∗dc_ave, and the input voltage average value Vin. $V^*_{dc\_ave}$ should be selected carefully so that the value of dSH does not become negative because of the double-frequency swing, and the summation of dSH and m is always smaller than 1. For different input voltages, $V^*_{dc\_ave}$ could be optimized to achieve lowest switching device voltage stress.

A feed-forward component $V^*_{c2}/V^*_{dc\_ave}$ is added to the output of the capacitor voltage controller to increase the dynamic performance. The DFR suppression controller is composed by one resonant controller whose frequency is designed at two times the grid frequency. The input of the controller is the DFR existed in v_{IN}. It equals to the difference between v_{IN} and V_{in}. The input DFR suppression controller ensures that the DFR in C1 and C2 does not flow into the input.

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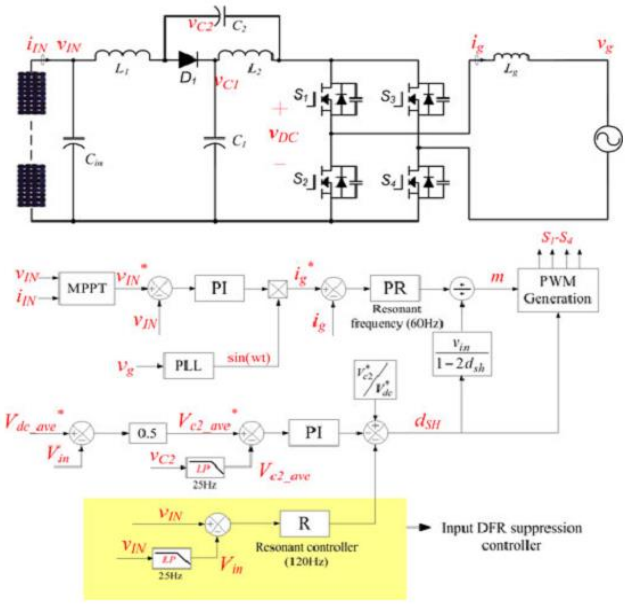

Fig. 3. Diagram of the proposed control system.

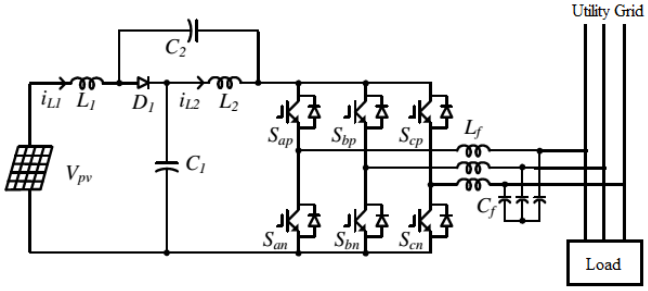

Fig 4. Quasi Z-Source Inverter for Grid Connected PV PCS

The key features of this proposed system are

- ✓ Single power stage for buck and boost, power inversion, and maximum power point tracking;
- ✓ Minimum number of switching devices;
- ✓ More reliable and lower cost; High immunity to EMI noise and high efficiency
- ✓ Reduced capacitance of inverter due to the use of Double-Frequency Ripple Suppression Control

III. CONTROL METHODS

A) Buck/Boost Conversion Mode

If the inverter is operated entirely in the non-shoot-through states (Fig. 3.5a) the diode will conduct and the voltage on capacitor C1will be equal to the input voltage while the voltage on capacitor C_2 will be zero. Therefore, $v_{PN} = V_{in}$ and the qZSI acts as a traditional VSI:

$$\hat{v}_{\ln} = \frac{\hat{v}_{PN}}{2} \cdot M = \frac{V_{in}}{2} \cdot M \qquad \text{……..2}$$

For SPWM $0 \le M \le 1$; and for SVPWM $0 \le M \le 2/\sqrt{3}$

Thus when D = 0, v_{ln} is always less than $V_{in}/\sqrt{3}$ and this is called the buck conversion mode of the qZSI. By keeping the six active states unchanged and replacing part or all of the two conventional zero states with shoot through states, one can boost $\hat{v}_{PN}$ by a factor of B, the value of which is related to the shoot-through duty ratio. This is called the boost conversion mode of the qZSI. The peak ac voltage becomes

$$\hat{v}_{\ln} = \frac{\hat{v}_{PN}}{2} \cdot M = \frac{V_{in}}{2} \cdot BM \qquad \text{……3}$$

B) Boost Control Methods

All the boost control methods that have been explored for the traditional ZSI (i.e. simple boost, maximum boost, maximum constant boost) [5-7] can be utilized for qZSI control in the same manner. Generally speaking, the voltage gain of the qZSI is

$$G = \hat{v}_{\ln} / 0.5\hat{v}_{PN} = MB \qquad \text{…..4}$$

Whereas the voltage stress across the inverter bridge is BV_{in}. In order to maximize the voltage gain and minimize the voltage stress on the inverter bridge, one needs to decrease the boost factor B and increase the modulation index M as much as possible. Fig. 3.6 shows the voltage gain versus the modulation index of these three boost control methods. All have significantly higher gain than traditional PWM methods. Among these three boost control methods, the maximum boost control makes the most use of the conventional zero states, so it has the maximum M and the minimum voltage stress across the inverter bridge with the same voltage gain. However, it has the drawback of low-frequency ripples on the passive components of the qZSI, which requires a larger volume and weight and higher cost inductor and capacitor in the qZSI network. The simple boost control has evenly spread shoot-through states, thus it doesn't involve low-frequency ripples associated with output frequency; but its voltage stress is the largest with a given G. The maximum constant boost control makes a compromise of the two mentioned boost control methods.

In the proposed PV power generation system, in order to lower the voltage stress on the inverter bridge and keep a high voltage gain, the maximum constant boost control with third harmonic injection was chosen as the control method. Fig. 3.6 shows the sketch map. At (1/6) third harmonic injection, the maximum modulation index) M = $(2/\sqrt{3})$ can be achieved. The shoot-through states are introduced into the switching cycle when the carrier is either greater than V_P or less than V_N, which is evenly spread in each switching cycle. Thus the qZSI network doesn't involve low-frequency ripples. In this case, the shoot-through duty ratio is

$$D = \frac{T_0}{T} = 1 - \frac{\sqrt{3}M}{2} \qquad \text…..5$$

The boost factor is

$$B = \frac{1}{1-2D} = \frac{1}{\sqrt{3}M - 1} \qquad \text…….6$$

And the voltage gain equals

$$G = MB = \frac{M}{\sqrt{3}M - 1} \qquad \text…….7$$

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The peak ac phase voltage can be calculated as

$$\hat{v}_{ln} = \frac{V_{in}}{2} G = \frac{MV_{in}}{2\sqrt{3}M - 2} \quad \ldots\ldots.8$$

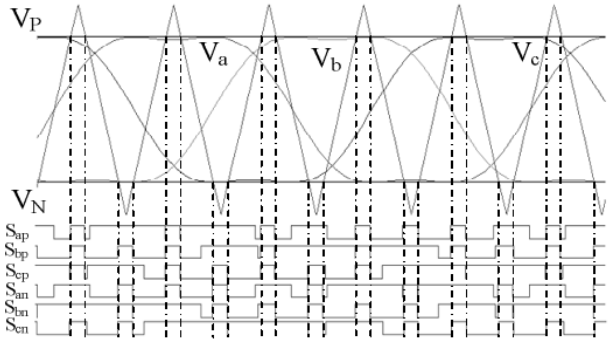

Fig 5. Sketch map of constant boost control for qZSI

IV. SIMULATION RESULTS

The proposed Double Deck buck boost converter performance is studied in MATLAB/SIMULINK platform. The fig 5(a), (b) shows the simulated circuit proposed converter. The Double Deck Buck Boost converter is implemented in wind power generation system. Wind power generation system produced electrical power with maximum voltage of 320V. The ac is rectified into dc using diode bridge rectifier, the dc voltage is 300V. This is given as input for the double deck buck boost converter and it is boosted to average value of 750V. The space vector PWM controlled three phase Voltage Source Inverter is used to convert dc into ac; the output rms voltage is 400V. The THD of inverter voltage is 5.60%.

Table 1. Simulation Parameters

Circuit Parameters	Value
Inductors L_1 and L_2	300µH
Inductor L_S	80µH
Capacitor C_O	200µF
Rectifier Capacitor	0.8mF
DC Bus Capacitor	400µF

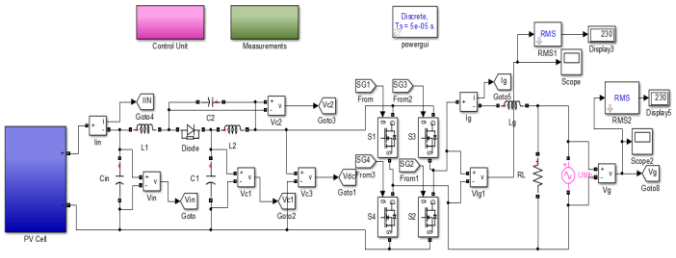

Fig 6. Simulation diagram of single phase grid connected qZSI with conventional control

The quasi z source inverter fed with photovoltaic input and output connected to local grid is simulated in MATLAB/Simulink. The 1kW solar PV array is modeled to produce 180volts dc. In the conventional method of generating control pulses constant Vp and Vn are used as shown in Fig 8.

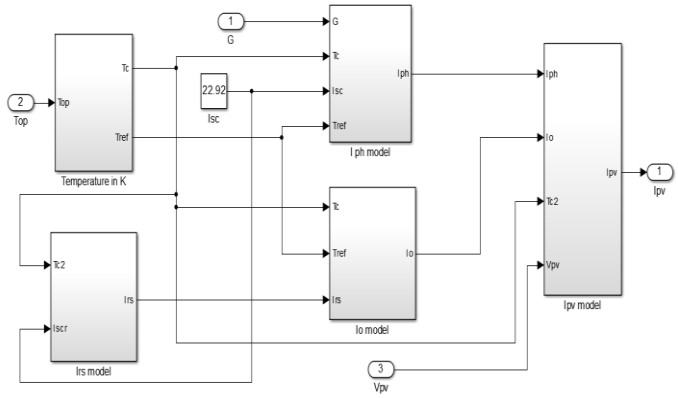

Fig 7. Simulation diagram of PV module modeling.

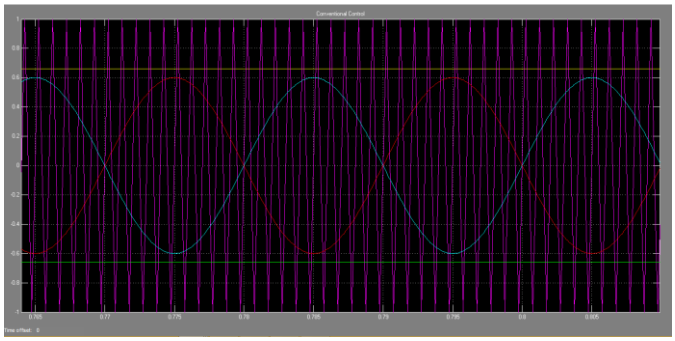

Fig 8. Conventional control signals

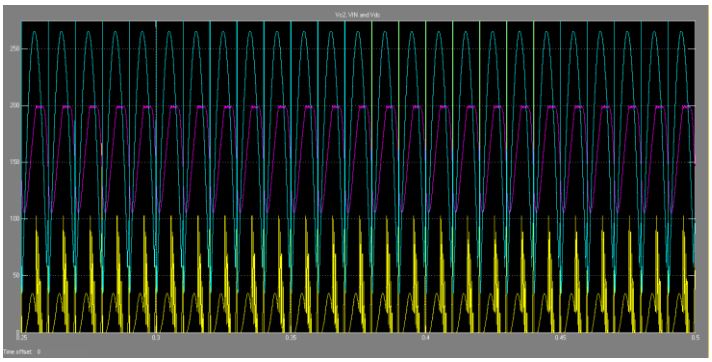

Fig 9. Vdc, V_{IN} and V_{C2} waveforms of the qZSI with the conventional control, C1 =800µF

In the conventional method of control the quasi z source inverter parameters L1 and L2 are 396µH and 258µH respectively and the C1 and C2 are 800µF and 28µF.

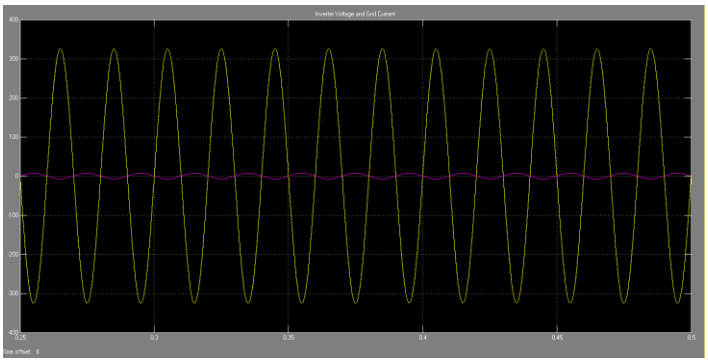

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Fig 10. qZSI output votage and grid current

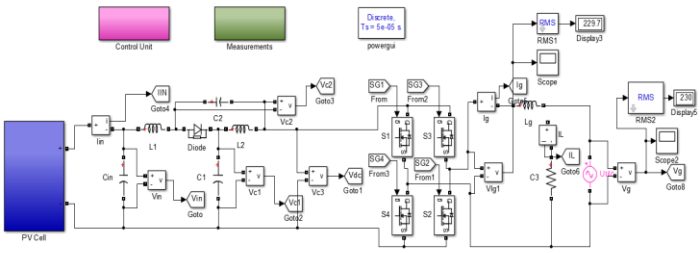

Fig 11. Simulation diagram of qZSI with proposed control

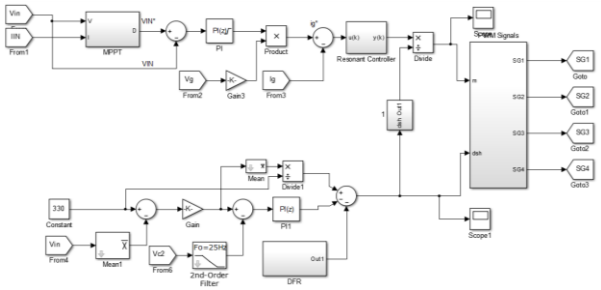

Fig 12. Simulation diagram of Proposed Double Frequency Ripple Suppression Control

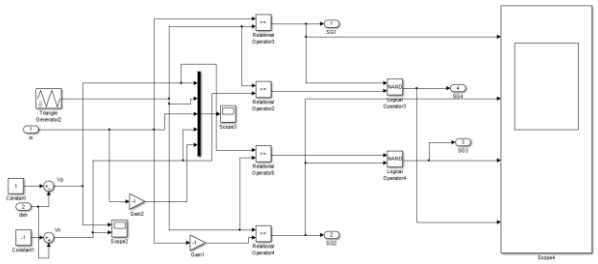

Fig 13. Simulation diagram of Gate signal generation

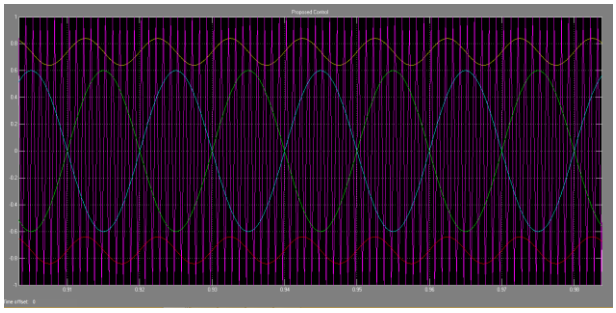

Fig 14. Simulation result showing proposed control mechanism

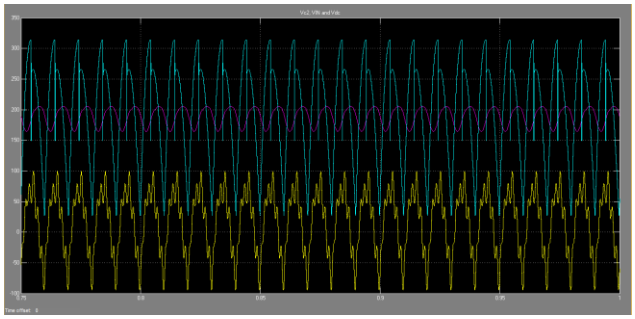

Fig 15. Vdc, V_{IN} and V_{C2} waveforms of the qZSI with the proposed control,C1 =100µF.

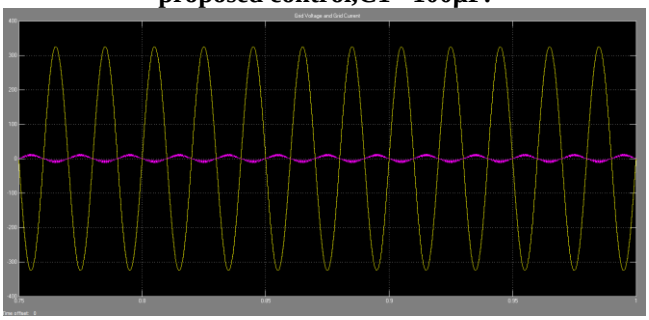

Fig 16. Simulation result of qZSI with proposed control

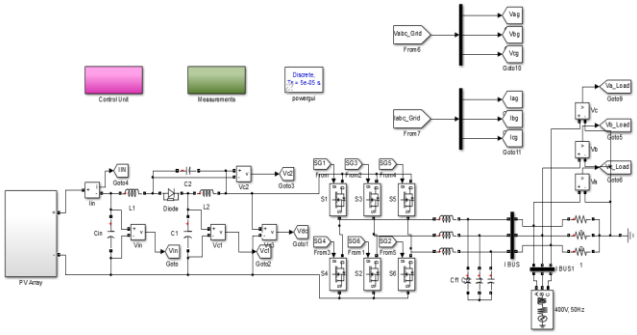

Fig 17. Simulation diagram of three phase qZSI with proposed control

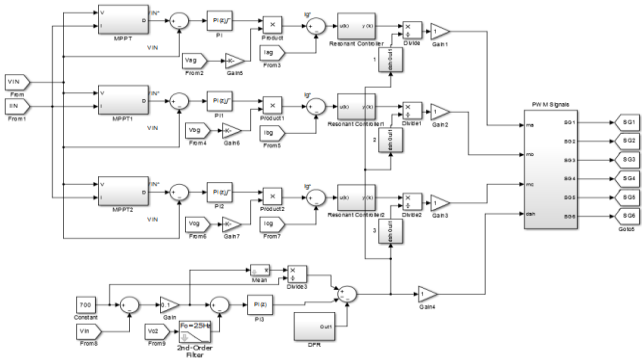

Fig. 18. Simulation diagram of DFR control for three phase circuit.

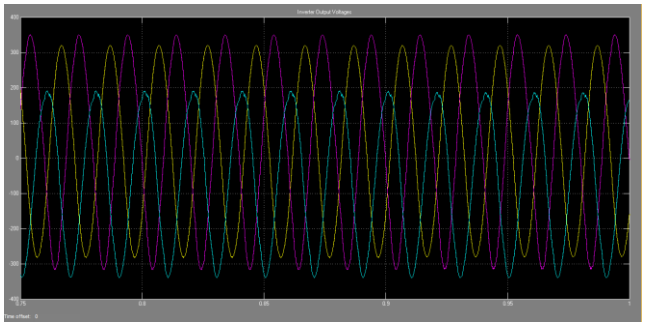

Fig 19. Three phase qZSI output voltages with proposed control

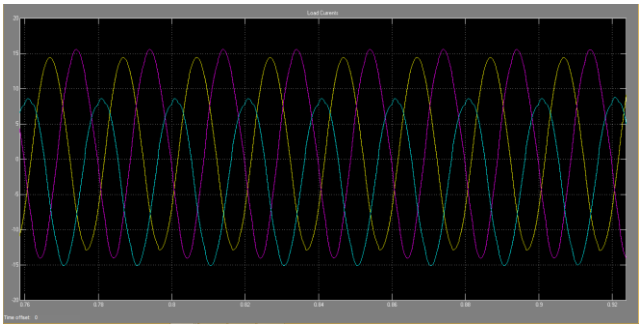

Fig 20. Three phase qZSI output currents to load with proposed control

V. CONCLUSION

In this project, a new control strategy is proposed to minimize the capacitance requirement in single-phase qZSI PV system and three phase system. Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the DFR energy. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability much. For the developed 1-kW quasi-Z-source PV system, 800μF capacitor can be replaced with a 100μF capacitor by using the proposed method. However, the voltage stress across the switching devices was increased by 50% compared with the conventional design. The increase of the switching device voltage stress is only 15% compared with conventional design.

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