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Design an Ultra Wideband Low Noise Amplifier at 6 GHz Applications

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***Abstract*—This paper presents a ultra wideband low noise amplifier for 6GHz Applications. This proposed LNA is the extension of inductively common source amplifier and in this design we used transistor multifingering techniques in order to reduce noise and improves gain. This LNA is simulated by using UMC .18um CMOS mixed signal/RF process in cadence virtuoso. In this design, used current source biasing, with power supply is 1.8v. LNA achieved gain 19dB and noise figure is 1.8dB at operating frequency range, and input & output return losses are -24dB & -15dB respectively, reverse isolation is -36dB and stability is 4, IIP3 is -10dBm, 1-dB compression point -17dBm and total power consumption is 9mw.**

Keywords—cascode source degeneration amplifier, current mirror, low noise amplifier, de-Q resistor, multifingring Techniques.

I. INTRODUCTION

Ultra wideband communication system is a new wireless communication system that transmits an extremely low signal power over an ultra bandwidth [1]. It has an ability to provide high data rate at low cost with relatively low power. In the wireless communication system, low noise amplifier is the first block in the receiver, so that the sensitivity and noise figure of receiver is highly depend upon the gain and noise figure of low noise amplifier, and overall performance of receiver is depend upon low noise amplifier, the design of the front end low noise amplifier is one the challenges in radio frequency (RF) receivers, which needs to provide good input impedance matching, enough power gain and low noise figure (NF) with the operating frequency range. Various CMOS UWB LNA design techniques had been reported for wideband communication application. The well –developed distributed amplifier provides impedance matching, flat gain over wide bandwidth, but they are power hungry and occupy large area for the use of on chip transmission line [2, 3]. The resistive-shunt feedback amplifiers provide wideband input matching, low noise figure using loop gain [4], but they are require large power to achieve a high loop gain in single stage. A common gate amplifier has the highest potential to achieve the wideband input matching, good linearity and input and output isolation, but it leads to lower gain and higher noise figure(NF) [5]. In this paper, a low noise amplifier for ultra wideband application was designed using .18um CMOS technology based on cascode source degeneration topology, in this design for reducing noise figure we used parallel combination of two NMOS transistor at output, and used a d-Q resistor parallel to drain inductor for stability purpose , so by using this techniques we got gain 19dB, noise figure 1.8dB, input and output return losses are -24dB & -15dB respectively, reverse isolation is -36dB and stability factor is 4, and power consumption is 9mw.

II. CIRCUIT DESIGN AND ANALYSIS

In the design of low noise amplifier there is tradeoff between different parameters i.e. gain, noise figure, power consumption, linearity, bandwidth, impedance matching, if we goes to improves some parameters, other parameter can be disturbed. So here my objective is to achieve higher gain with minimum noise figure.

Noise figure (NF)

According to friss formula overall noise figure of n-stage receiver is-

$$\mathrm{NF_{tot}} = 1 + (\mathrm{NF_1} - 1) + \frac{(\mathrm{NF_2} - 1)}{\mathrm{A_1}} + \cdots \frac{(\mathrm{NF_n} - 1)}{\mathrm{A_1} \ldots \ldots \mathrm{A_{(n-1)}}}$$

Here $\mathrm{A_1}$ is the gain of first stage and it is usually high, we can discard the noise contribution of the later stages on overall noise calculation , that is why we concentrates only on the noise of M1, which is shown in fig.1.

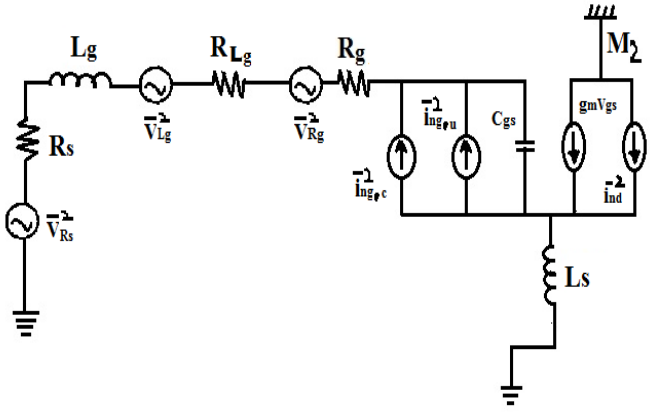

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Figure 1

The noise figure is the ratio between the total output noise power due to all noise sources and the output noise power generated by the input source [5].

The input stage of M1

$$NF = \frac{\overline{V_{Rs}}^2 + \overline{V_{Rg}}^2 + \overline{V_{Lg}}^2 + \overline{V_{nd}}^2}{\overline{V_{Rs}}^2}$$

It contains current noise in drain ($\overline{\iota_{nd}}^2$), current noise in gate ($\overline{\iota_{ng}^2} = \overline{\iota_{ng,c}^2} + \overline{\iota_{ng,u}^2}$), resistance noise from R_g and L_g ($\overline{\iota_{Rg}^2}$ and $\overline{\iota_{Lg}^2}$). Here we are using power constrained noise optimization techniques this gives a specified bound on power consumption, this method then yield the optimum width that minimizes noise. So the noise figure of such device is:-

$$\mathrm{NF} = 1 + \frac{\mathrm{R_{Lg}}}{\mathrm{R_s}} + \frac{\mathrm{R_g}}{\mathrm{R_s}} + \frac{\gamma\chi}{\chi \mathrm{Q_L}}\left(\frac{\omega_0}{\omega_\mathrm{T}}\right)^2$$

γ Is the thermal noise in the channel of M1, $\alpha = \frac{g_{m1}}{g_{d01}}$ (α =1 in long channel device), Q_L is the quality factor of input match network and equal to $\frac{1}{\omega_0 R_S C_{gs1}}$, ω_0 is the operating frequency and $\omega_T = \frac{g_{m1}}{c_{gs1}}$ is the unity gain frequency.

Optimum Value of Q_L for power constrained noise optimization:

$$Q_{L,opt,pd} = |C|\sqrt{\frac{5\gamma}{\delta}}\left[1 + \sqrt{1 + \frac{3}{|c|^2}\left(1 + \frac{\delta}{5\gamma}\right)}\right] \approx 3.9$$

So, minimum noise figure is-

$$\mathrm{NF_{min,pd}} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_\mathrm{T}}\right)$$

Input impedance match

From the fig. 1 the input impedance of LNA is $Z_{in} = sL_g + R_{Lg} + R_g + sL_s + \frac{1}{sC_{gs1}} + \omega_T L_s$, we can equal these input impedance to source impedance of 50Ω, for the simplification neglect the value of R_{Lg} and R_g , then $\omega_T L_s = R_s \rightarrow L_s = \frac{R_s}{\omega_T}$ and $L_g = \frac{1}{\omega_0^2 C_{gs1}} - L_s$

Gain

In low noise amplifier there is a several types of gain i.e. operating power gain, transducer power gain, and available power gain. Operating power gain G_P is the ratio of power delivered to the load to power supplied to amplifier, transducer power gain G_T is the ratio of maximum power available from source to power delivered to load;

Available power gain G_A is the ratio of power available from the source to power available from the amplifier

$$G_p = \frac{1}{1 - |\Gamma_{in}|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - (S_{12}S_{21}\Gamma_S\Gamma_L)|^2}$$

$$\mathrm{G_A} = \frac{1 - |\mathrm{S_{11}}|^2}{|1 - \mathrm{S_{11}}\Gamma_\mathrm{S}|^2}|\mathrm{S_{21}}|^{\backslash 2}\frac{1}{|1 - \mathrm{S_{22}}\Gamma_\mathrm{L}|^2}$$

Γ_{in} Represents the input reflection coefficient, Γ_S represents the source reflection coefficient, Γ_L represents load reflection coefficient.

Circuit design

The overall performance of the low noise amplifier is determined by calculating the transducer gain, noise figure and input and output reflection coefficients. The complete schematic design of low noise amplifier is shown in figure 2. Transistor M1 is common source degeneration amplifier and M2, M3 are common gate amplifier, by using these cascode network reverse isolation is improved, $C_{in}$is the input dc blocking capacitor, C_o is output blocking capacitor, L_S is source degeneration inductor is used to give the input matching and high input impedance, L_g is gate inductor used to tune out the effect of C_{in} and set the resonant frequency, L_d is drain inductor used to tuned the output and increase gain and also work as a band pass filter form with C_o. R_d resistance is d-Q resistor are connected parallel to drain inductor in order to increase stability. R_{ref} and R_{bias} is the part of biasing network. The calculated width of M1 is 130um but we chosen width of M1 is 100um, M2=M3 is 50um and M5 is 5um. The components values are given in table 1. Here inductor Lg, Lsand Ld are on chip spiral inductor .

Proposed Circuit of LNA: This schematic circuit is designed by using cadence tool.

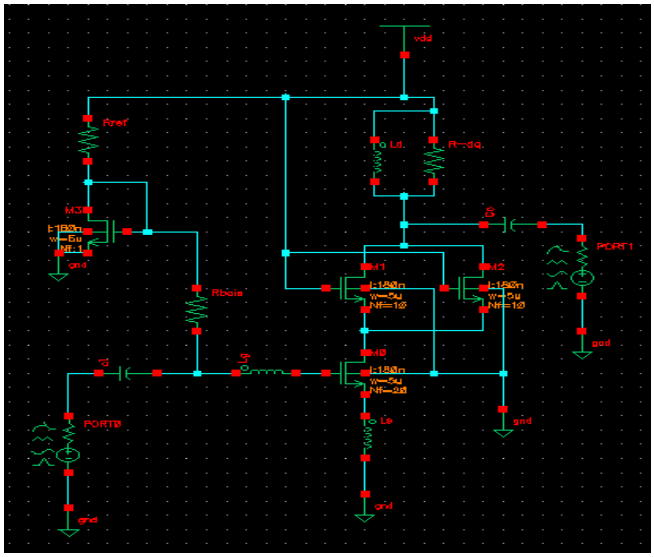

Figure:2 Schematic Diagram of LNA

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The values of the components are-

Components	Lg	Ls	Ld	Rbias	Rref	Cin	Cout	Rs	Vdd
Value	3.39nH	200pH	2.8nH	2.4K	2.4K	2pF	130fF	50Ω	1.8v

Table.1

III. SIMULATION RESULT

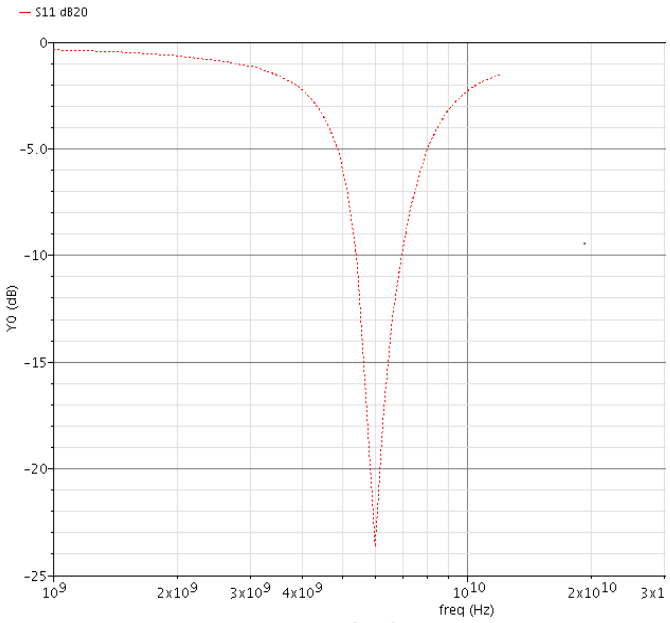

Figure 3.1 S11

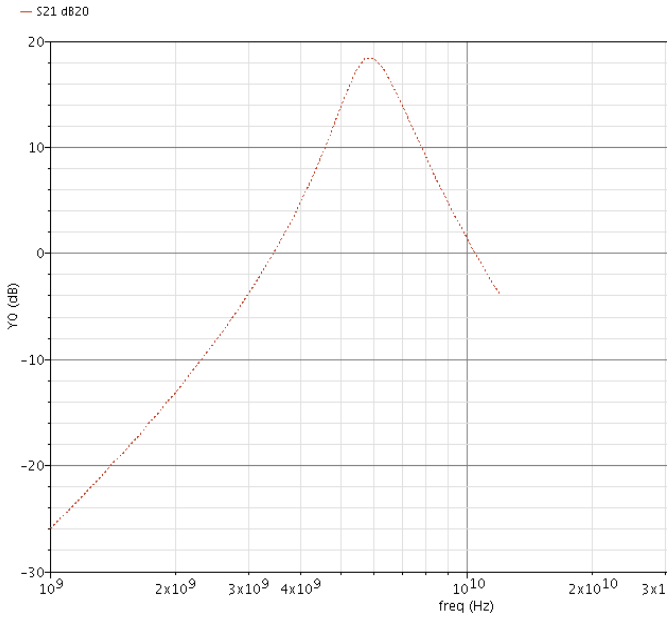

Figure 3.3 S21

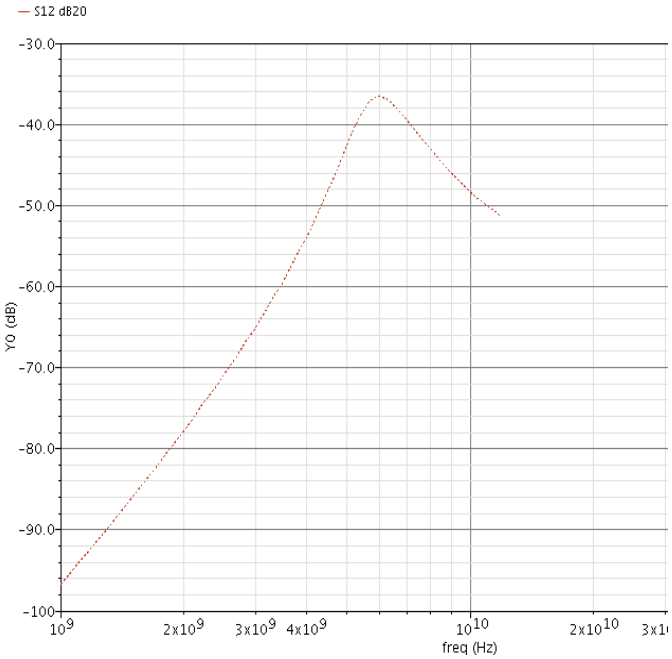

Figure 3.2 S12

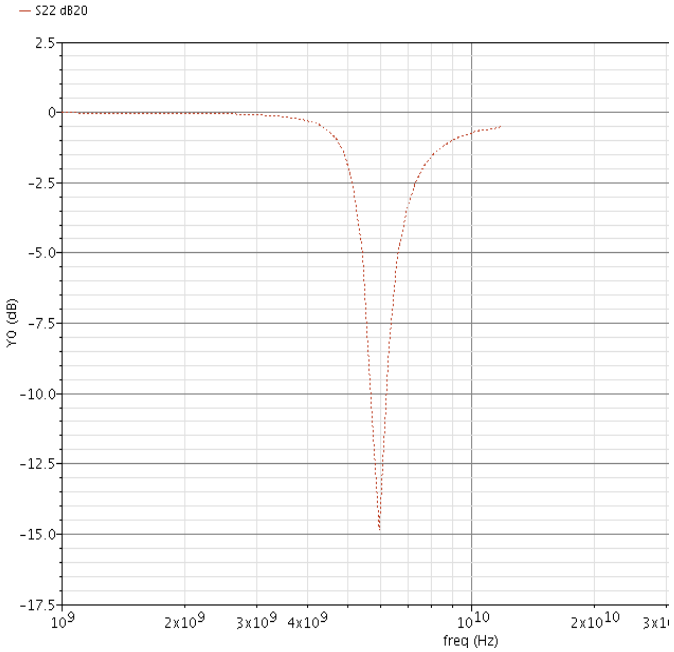

Figure 3.4 S22

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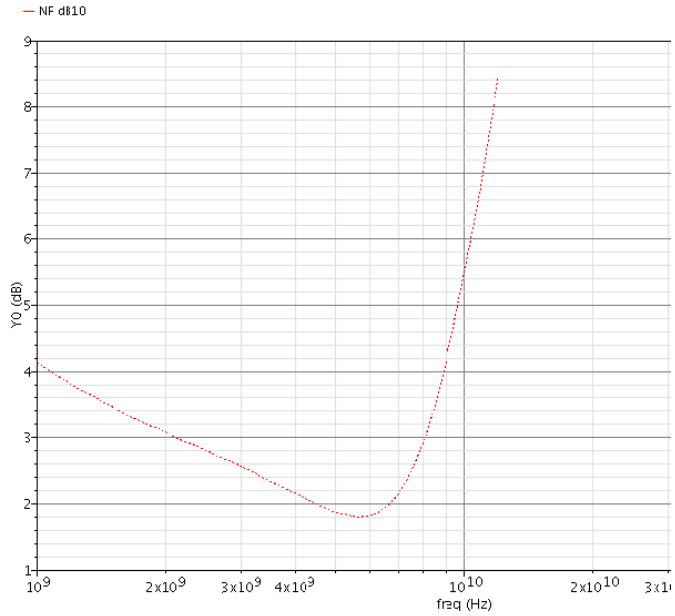

Figure 3.5 NF

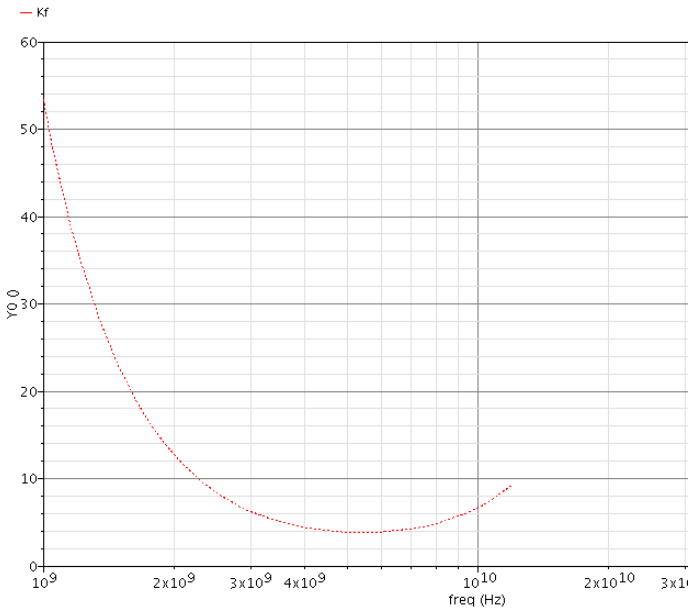

Figure 3.6 Kf

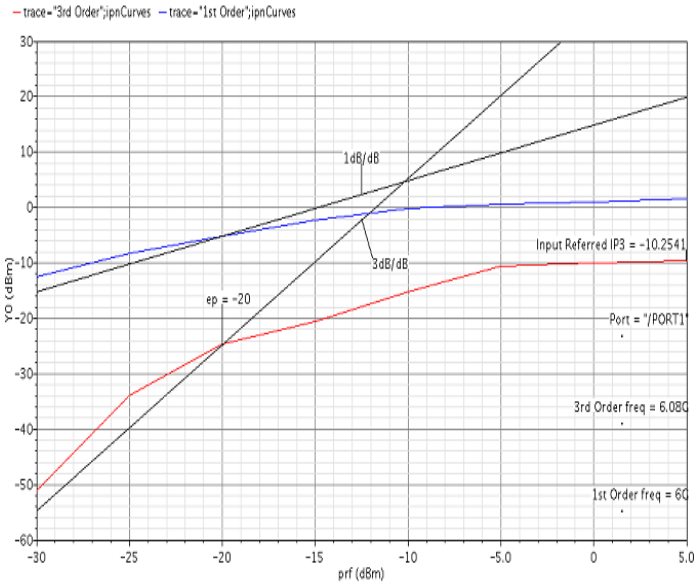

Figure 3.7 IIP3

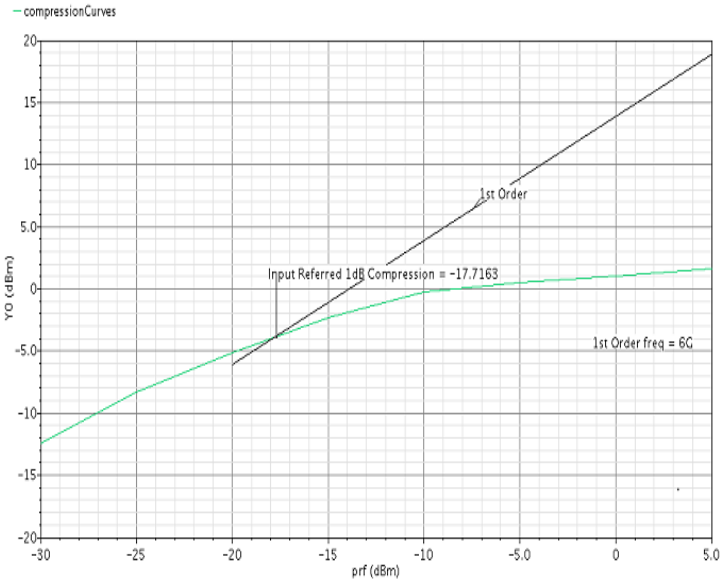

Figure 3.8 1dB Compression point

RESULT TABLE

Frequency (GHz)	S_{11}(dB)	S_{12}(dB)	S_{21}(dB)	S_{22}(dB)	NF(dB)	K_f	IIP3(dBm)	1 dB Compression point(dBm)
6	--24	-36	18.53	-15	1.8	4	-10.25	-17.7

Table 2

III. CONCLUSION

As we know low noise amplifier is the crucial part in RF receiver. In this paper design the low noise amplifier at 6GHz operating frequency, it has stimulated by using cadence for this design and it offers improved gain, good reverse isolation and reduced miller effect, this LNA recorded the Virtuoso tool by using .18um CMOS Technology, we have chosen cascode topology with source degeneration

amplifier gain S_{21} is 18.53dB and the return loss S_{11} and S_{22} is -24dB and -15dB, reverse isolation is -36dB noise figure is 1.8dB, stability factor K_f is 4 , power consumption is 9mw.

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