www.ijecs.in
International Journal Of Engineering And Computer Science ISSN:2319-7242
Volume 3, Issue 10 October, 2014 Page No. 8888-8896

Comparison of Selective Harmonic Elimination And Space Vector PWM for Common-Mode Voltage Reduction in Three-Level Neutral-Point-Clamped Inverters for Variable Speed Induction Drives

Gangadhara Swamy[1], Nomula Ganesh..[2]
[1] M.Tech Student
Siddhartha Institute of Technology & Science
Hyderabad,India

[2] Associate prof , M.Tech
. Siddhartha Institute of Technology & Science
Hyderabad,India

Abstract—This paper proposes a hybrid selective harmonic elimination pulsewidth modulation (SHEPWM) scheme for common mode voltage reduction in three-level neutral-point-clamped inverter-based induction motor drives. The scheme uses the conventional SHEPWM (C-SHEPWM) to control the inverter at high frequency (≥ 0.9 motor rated frequency) and uses the modified SHEPWM (M-SHEPWM) to control the inverter at low frequency. It also uses a scheme to ensure the smooth transition between the two SHEPWM schemes. As a result, at high frequency, the C-SHEPWM provides the required high modulation index for the motor, while at low frequency, when a passive filter is less effective for common-mode voltage reduction, the M-SHEPWM is used to suppress the common-mode voltage. Experimental results show that the proposed hybrid SHEPWM scheme could meet the modulation index need of the motor and reduce the common-mode voltage in the drive, and the two SHEPWM schemes could transition smoothly.

***Index Terms*—Bearing current, common-mode voltage (CMV), selective harmonic elimination pulsewidth modulation (SHEPWM), three-level inverter**

INTRODUCTION

Three-level neutral-point-clamped (NPC) inverters are used to drive medium-voltage high-power ac motors because of their high-voltage and high-power capacity and excellent harmonic performance. Such motor drives are used in many high-power variable-speed applications, such as highpower pumps and fans, leading to significant energy savings [1].

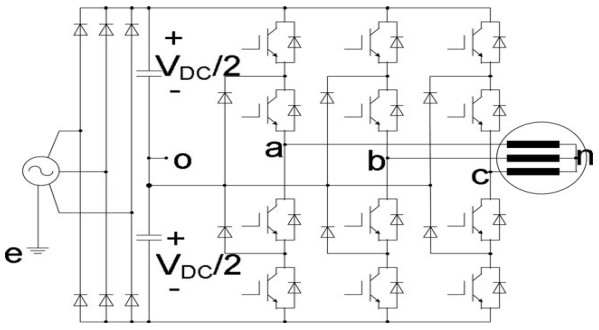

Fig. 1. Circuit diagram of three-level NPC induction motor drive with front- end diode rectifier.

Despite their different advantages, similar to two-level inverters for low-voltage ac motor drives, three-level NPC inverters generate common-mode voltage (CMV). The CMV in a threelevel NPC induction motor drive with a front-end diode rectifier is shown in Fig. 1. The CMV is defined as the voltage between the neutral point of the motor (node *n*) and the earth ground (node *e*), i.e., *Vne*. *Vne* can be decomposed into two voltages: one is the voltage from the neutral point of the motor to the mid-point of the dc link, i.e., *Vno* and the other is the voltage

from the mid-point of the dc link to the earth ground, i.e., *Voe* . Both *Voe* and *Vno* are ac voltages. *Voe* depends on the connection and grounding of the input AC source [2]. For example, if the input ac source is in the Y-connection and the neutral point of the Y-connection is grounded, *Voe* is close to a sinusoidal voltage whose frequency is three times the frequency of the input ac source and whose peak value is about 10% of the dc-link voltage [2]; if the input ac source is in the Δ-connection and one corner of the Δ-connection is grounded, *Voe* will have twice higher peak value but twice lower frequency [2]. *Vno* is related to the output voltage of the inverter legs (*Vao* , *Vbo* , and *Vco*) as

$$V_{no} = \frac{V_{ao} + V_{bo} + V_{co}}{3}. \quad (1)$$

In a pulsewidth modulated (PWM) controlled inverter, each inverter leg output voltage is a PWMmodulated step-wise voltage. represented with the Fourier series, such a voltage contains the fundamental voltage for the motor as

well as different harmonic terms, including the harmonics at multiples of the carrier frequency, the harmonics in the sidebands around the carrier frequency and multiples of the carrier frequency [3], [4], and the high-frequency harmonics due to the step-change that are blamed for the electromagnetic interference (EMI) problem. As a result, *Vno* is also a step-wise voltage that contains many harmonics, though some three-phase balanced voltage terms in *Vao* , *Vbo* , and *Vco* are canceled out in *Vno*.

As a combination of *Vno* and *Voe* , *Vne* contains harmonic voltage from both *Vno* and *Voe* . Many of the harmonics in *Vne* can couple through different stay capacitances in the motor, such as the stray capacitance between the stator winding and the grounded stator core, the stray capacitance between the stator winding and the rotor core, and the stray capacitance between the inner race of the bearing and the grounded stator core, to
cause a voltage across the bearing and hence a current through the bearing. Such a bearing current can affect the properties of the bearing lubricant and cause bearing electroerosion [5]. Different harmonics in *Vne* can also cause a current to flow through the stray capacitance between the stator winding and the grounded stator core and other ground conductors. Such a ground current can trip the ground current relays that are used to protect the drive [6]. The aforementioned currents also cause losses in the drive and the EMI problem [7], [8].

A solution to the CMV problem is to use filters [8]–[10] to reduce the CMV or the common-mode current. The solution is effective and does not require modifications of the PWM control strategy. However, the filters increase the size, weight, and cost of the drive, though the increase is acceptable in some applications.

The other solution is to revise the PWM control strategy for the inverter to reduce the CMV *Vne*. Since *Voe* depends on the connection and grounding of the input ac source, the proposed solutions focus on using modified PWM control strategies to reduce *Vno*. The solution proposed in [2] uses a modified space vector PWM (SVPWM) scheme to reduce *Vno*. An SVPWM scheme takes advantages of the fact that the output voltage of an inverter leg only has three levels (*V*DC/2, 0, −*V*DC/2) or three states (denoted as "1," "0," and "−1," respectively), and therefore, the inverter only has 33 = 27 possible states or space vectors, which are shown in Fig. 2. Unlike the conventional SVPWM (C-SVPWM) scheme, which uses all 27 space vectors to synthesize the reference voltage vector, this solution uses only 19 switching states to synthesize the reference space vector. The other eight switching states that lead to large (• }*V*DC/3 or • }*V*DC/2) *Vno*, i.e., (1,1,0), (1,0,1), (0,1,1), (−1, −1,0), (−1,0, −1), (0, −1, −1), (1,1,1), and (−1, −1, −1), are discarded. The method reduces the magnitude of *Vno* to *V*DC/6 from *V*DC/2 in the C-SVPWM. However, the method uses the same number of transitions in each PWM cycle as the C-SVPWM, which limits its effectiveness in reducing the common-mode current in the 150 KHz–30MHz frequency range for the electromagnetic compatibility (EMC) standard in conducted emissions. The solution proposed in [11] uses only 7 out of the 27 space vectors, i.e., (0,1,−1), (1,0,−1), (1,−1,0), (0,−1,1), (−1,0,1), (−1,1,0), and (0,0,0), to synthesize the reference vector. Since each of the seven space vectors leads to zero motor neutral point to dc-link mid-point voltage *Vno*, the method can tremendously reduce the CMV. However, the method has reduced modulation index (up to 1 rather than 1.15 in a C-SVPWM) and harmonic performance. A revised carrier-based PWM is also proposed in [11] to reduce the CMV. The method uses three balanced sinusoidal modulation signals, i.e., *Vm*1 , *Vm*2 , and *Vm*3 , to compare with a triangle carrier signal to yield three intermediate PWM signals *V*1 , *V*2 , and *V*3 . Then, the method uses (*V*1 − V2), (*V*2 − *V*3), and (*V*3 − *V*1) as the PWM signals for the three phases of the inverter. As a result, the motor neutral point to dc-link midpoint

voltage is $[(V_1 - V_2) + (V_2 - V_3) + (V_3 - V_1)]/3 = 0$.

However, the method also has reduced modulation index (up to 0.87). Another revised carrier-based PWM is proposed in [12] and [13]. The method uses the discontinuousPWMand synchronized switching to reduce the number of inverter commutations and therefore the number of *Vno* pulses in one switching period.

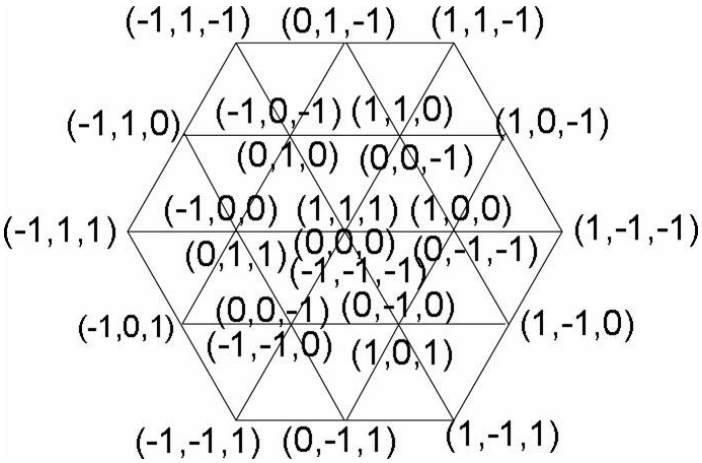

Fig. 2. Vector Diagram of Three-Level NPC Inverter.

As a result, the method reduces the common-mode current in the 150 KHz–30MHz frequency range for the EMC standard in conducted emissions. However, the method does not reduce the magnitude of *Vno*, which limits its effectiveness in reducing the magnitude of the common-mode current at lower frequency.

The aforementioned PWM schemes for CMV or commonmode current reduction are based on SVPWM or carrier-based PWM. The use of another popular PWM scheme, selective harmonic elimination PWM (SHEPWM), for CMV or common current reduction in three-level NPC inverters, has not been adequately explored. The advantages of SHEPWM include direct control over output harmonics [14], reduction of switching frequency and therefore switching loss [15], possibility of overmodulation [15], and high power quality [15], [16].

This paper investigates the use of SHEPWM for CMV reduction in three-level NPC inverters. The fundamental principle of the proposed SHEPWM scheme is discussed

in Section II. The experimental results are presented in Section III. The conclusions are drawn in Section IV.

II. PROPOSED SHEPWM SCHEME

An SHEPWM scheme describes the output voltage of each inverter leg with a Fourier series and shapes the inverter leg output voltage properly, so that unwanted harmonics are eliminated from the Fourier series. To this end, an SHEPWM scheme usually shapes the output voltage of each inverter leg into a quarter-wave symmetric waveform, so that even harmonics
are eliminated from the Fourier series. A typical quarter-wave symmetric waveform for an inverter leg output voltage is shown

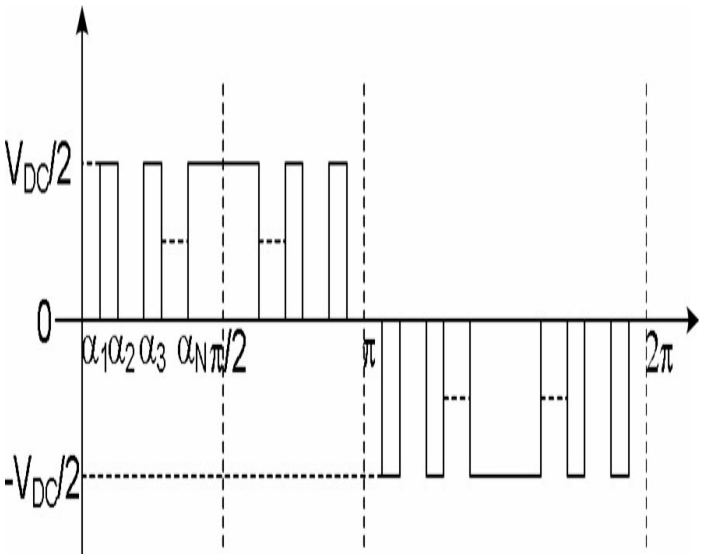

Fig. 3. Typical quarter-wave symmetric output voltage of a three-level NPC inverter leg.

in Fig. 3, where $\alpha 1$, $\alpha 2$, . . ., αN are the phase angles in a fundamental cycle where the inverter leg is switched or commutated. The Fourier series of such a voltage is given as [14], [15]

$$V_{xo} = \sum_{m=1}^{\infty} d_m \sin(m\omega t), \quad m = 1, 2, 3, \ldots \tag{2}$$

where *Vxo* is the output voltage of an inverter leg, *x* = *a*, *b*, or
c; *dm* is given as

$$d_m = \begin{cases} 0, & \text{when } m \text{ is even} \\ \dfrac{2V_{\mathrm{DC}}}{m\pi} \displaystyle\sum_{k=1}^{N} (-1)^{k+1} \cos(m\alpha_k), & \text{when } m \text{ is odd.} \end{cases} \tag{3}$$

An SHEPWM scheme also finds proper $\alpha 1$, $\alpha 2$, . . ., αN values to eliminate selected odd harmonics from the Fourier series. For example, if the 5th, 7th, 11th, and 13th harmonics are to be eliminated, $d5$, $d7$, $d11$, and $d13$ can be calculated according to (3) as

$$d_5 = \frac{2V_{\mathrm{DC}}}{5\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(5\alpha_k) \tag{4}$$

$$d_7 = \frac{2V_{\mathrm{DC}}}{7\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(7\alpha_k) \tag{5}$$

$$d_{11} = \frac{2V_{\mathrm{DC}}}{11\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(11\alpha_k) \tag{6}$$

$$d_{13} = \frac{2V_{\mathrm{DC}}}{13\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(13\alpha_k). \tag{7}$$

The resultants $d5$, $d7$, $d11$, and $d13$ are then set to zero to yield the following equations

$$\frac{2V_{\mathrm{DC}}}{5\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(5\alpha_k) = 0 \tag{8}$$

$$\frac{2V_{\mathrm{DC}}}{7\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(7\alpha_k) = 0 \tag{9}$$

$$\frac{2V_{\mathrm{DC}}}{11\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(11\alpha_k) = 0 \tag{10}$$

$$\frac{2V_{\mathrm{DC}}}{13\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(13\alpha_k) = 0. \tag{11}$$

TABLE I
FEATURES OF C-SHEPWM AND M-SHEPWM

	C-SHEPWM	M-SHEPWM
Harmonics eliminated	$6k\pm1$	$4k\pm1$
Maximum modulation index	1.15	1
Highest harmonic order eliminated	$3N$ - 2	$2N$ - 1

Solving (8)–(11) for $\alpha 1$, $\alpha 2$, . . ., αN will yield $\alpha 1$, $\alpha 2$, . . ., αN values and therefore switching moments for the inverter leg that lead to cancellation of the 5th, 7th, 11th, and 13th harmonics from the Fourier series. Of course, the number of the harmonic terms or the highest order

harmonic term that can be eliminated depends on the *N* value; a larger *N* value will allow more harmonic terms or a higher order harmonic term to be eliminated.

The aforementioned transcendental equations can be solved with a certain iterative method, such as the Newton method. Such methods have been discussed extensively in the literature [15], [17]–[19].

One commonly used SHEPWM scheme, termed as C-SHEPWM in [20], eliminates (6*k* • *}* 1)th (5th, 7th, 11th, 13th, . . .) harmonics, while keeping triplen harmonics in each inverter leg output voltage. This SHEPWM scheme takes advantage of the fact that the triplen harmonics, though existing in the inverter leg output voltage, will be canceled in the line-to-line voltage of the motor. Because of the presence of the third harmonic in each inverter leg output voltage, similar to carrier-based PWM with the third harmonic injection, this SHEPWM scheme has a high modulation index of 1.15. However, the triplen harmonics produces CMV, as shown by (1).

Another SHEPWM, termed as modified SHEPWM or M-SHEPWM in this paper and improved SHEPWM in [20], eliminates (4*k* • *}* 1)th (3rd, 5th, 7th, 9th, . . .) harmonics. Since this SHEPWM scheme eliminates low-order triplen harmonics from each inverter leg output voltage, it reduces the CMV of the inverter. However, it has reduced modulation index (up to 1) because of absence of the third harmonic in each inverter leg output voltage. Also, the highest harmonic term that can be eliminated in M-SHEPWM is lower than in C-SHEPWM. The features of C-SHEPWM and M-SHEPWM are summarized in Table I.

This paper proposes a hybrid SHEPWM scheme that takes advantage of the features of both the C-SHEPWM and the M-SHEPWM. The proposed SHEPWM uses the C-SHEPWM to control the inverter at high frequency (≥ 0.9 motor rated frequency) and the M-SHEPWM at low frequency. As a result, at high frequency, the proposed SHEPWM provides high modulation index and therefore high voltage for the motor, which is crucial for high-frequency (high-speed) operation of the motor. Though the C-SHEPWM produces higher CMV, since the operating frequency and therefore the frequency of the CMV is high, a low-pass filter that consists of inductors in series with the motor and capacitors in parallel with the motor can effectively suppress theCMVor common-mode current of the motor. At low frequency, where the common-mode filter is less effective for CMV reduction, the M-SHEPWM is used to reduce the CMV. Though the M-SHEPWM offers a reduced modulation index, such a modulation index is sufficient for low-frequency operation of the motor.

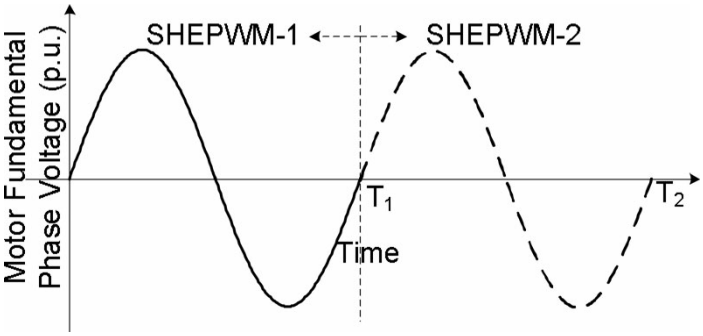

Fig. 4. Transition between C-SHEPWM and M-SHEPWM.

When the motor frequency crosses the boundary between the high and low frequencies, the C-SHEPWM and the MSHEPWM will transition from one to the other. To ensure the smooth transition between the twoSHEPWMschemes, the transition is done only when the fundamental motor phase voltage completes a full cycle and passes the zero-crossing point, as shown in Fig. 4. The first SHEPWM (SHEPWM-1) continues to be used until the fundamental motor phase voltage completes a full cycle and passes the zero-crossing point at the moment*T*1 , after which the second SHEPWM (SHEPWM-2) is used to run the inverter.

III. SIMULATION RESULTS OF SHEPWM

The proposed hybrid SHEPWM scheme has been tested on a three-level NPC inverter. The inverter was built for a 50-Hz, 380-V, 55-kW induction motor for an industrial pump application, where the motor constantly runs between 40 and 50 Hz. The inverter was tested along with the motor and the pump in the field. The constant *v*/*f* control scheme and the C SHEPWM were used to control the drive and provided satisfactory drive performance. The aforementioned *LC* low-pass filterwas used to suppress theCMVor common-mode current. The filterwas cool at high frequency (≥0.9 motor rated frequency or 45–50 Hz) but became hot at low frequency (0.8–0.9 motor rated frequency or 40–45 Hz) at the same ambient temperature. This is because the filter was less effective in reducing the common-mode current at low frequency, and therefore, larger common-mode current flew through the filter at low frequency.

Using a larger common-mode filter could lower the temperature of the filter at low frequency. However, it would increase the size and cost of the drive. The proposed hybrid SHEPWM

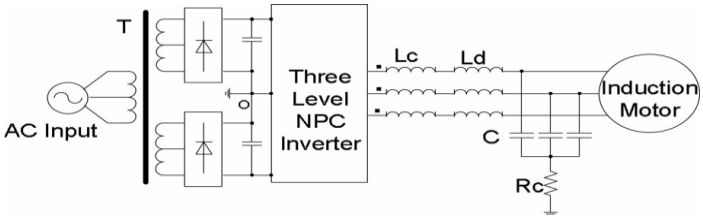

Fig. 5. Block diagram of tested induction drive.

schemewas used to reduce the CMVand therefore the commonmode current and hence the temperature of the filter at low frequency (40–45 Hz). The scheme was tested

in the lab. Because the inverter could be installed in the lab but the field motor could not, the scheme was tested on the aforementioned inverter and a scaled down induction motor.

The topology of the tested system is shown in Fig. 5. A transformer *T* with two separate secondary windings provided two separate ac inputs to two diode rectifiers (such a transformer was also available and used in the field). The two diode rectifiers were connected in series to provide a 600-V dc-link voltage and a stable neutral point (node O in Fig. 5) to the three-level NPC inverter. A passive filter made of a common-mode inductor *Lc* , a differential mode inductor *Ld* , a capacitor *C*, and a resister *Rc* was used to suppress the common mode as well as the differential mode noise, with *Lc* and *Rc* exclusively used for common-mode noise reduction, *Ld* primarily used for differential mode noise reduction and partially used for common-mode noise reduction, and *C* used for both common-mode and differential-mode noise reduction. *Lc* and *Ld* , which are in series connection with the motor, increase the overall impedance of the circuit where the common-mode current flows and therefore reduces the common-mode current; *C*, which is in parallel connection with the motor, shunts some of the common-mode current to the ground and therefore further reduces the common-mode current through the motor. *R* is a small resistor used to prevent resonance in the circuit. Increasing *Lc* , *Ld* , and *C* values will reduce the common-mode current but increase the size of the filter. Increasing the *C* value will also increase the leakage current into the ground. The following values for *Lc* , *Ld* , *C*, and *R* were used in the developed drive for good compromise between common-mode current reduction and the size and cost of the filter: *Lc* = 400 mH, *Ld* = 10 mH, *C* = 64 μF, and *Rc* = 3.9 Ω. The motor was a 3-kW, 50-Hz, 380-V (line–line voltage), Y connected induction motor. There was no other mechanical load on the shaft of the motor, except friction and windage in the motor and inertia on the shaft. The M-SHEPWM was used to control the inverter at 40–45 Hz and the C-SHEPWM was used at 45–50 Hz. Nine switching angles were used in each quarter fundamental cycle (*N* = 9), which means the highest switching frequency was 900 Hz.

The voltage from the neutral point of the motor to the midpoint of the dc link was tested at different frequency and with and without the passive filter. The test results are shown in

Figs. 6–13. Figs. 6 and 7 show the waveform and the spectrum of the voltage at 50 Hz without the passive filter, while Figs. 8 and 9 show the waveform and spectrum of the voltage at 50 Hz with the passive filter. Comparison of Figs. 6 and 8 shows that though the C-SHEPWM generated significant CMV, the CMV could be effectively suppressed by the filter because of the high operating frequency of the drive; the peak value of the motor neutral point to dc-link mid-pint voltage was reduced to 40 from 190V by the filter. Note different scales were used in Figs. 6 and 8 for clarity. Comparison of Figs. 7 and 9 also clearly shows the effectiveness of the filter in reducing the CMVat this frequencymany harmonic terms was cleared, and the peak values of the remaining harmonic terms were significantly reduced by the filter. Note different scales were also used in Figs. 7 and 9. Figs. 10 and 11 show the waveform and the spectrum of the voltage at 40 Hz without the passive filter, while Figs. 12 and 13 show the waveform and the spectrum of the voltage

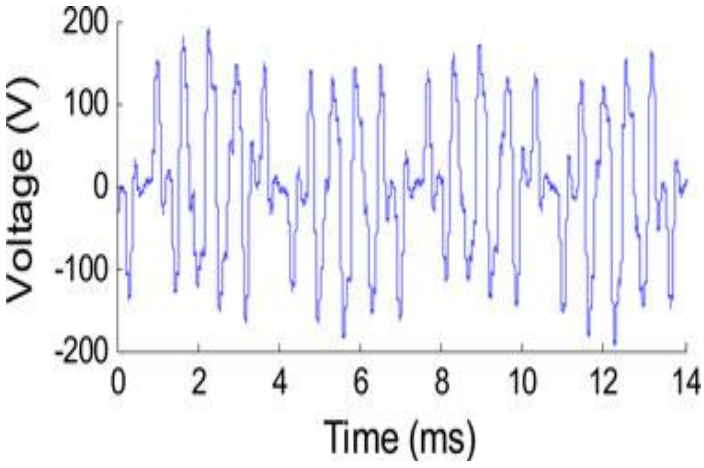

Fig. 6. Waveform of motor neutral point to dc-link mid-point voltage (100 V/Div) at 50 Hz without passive filter.

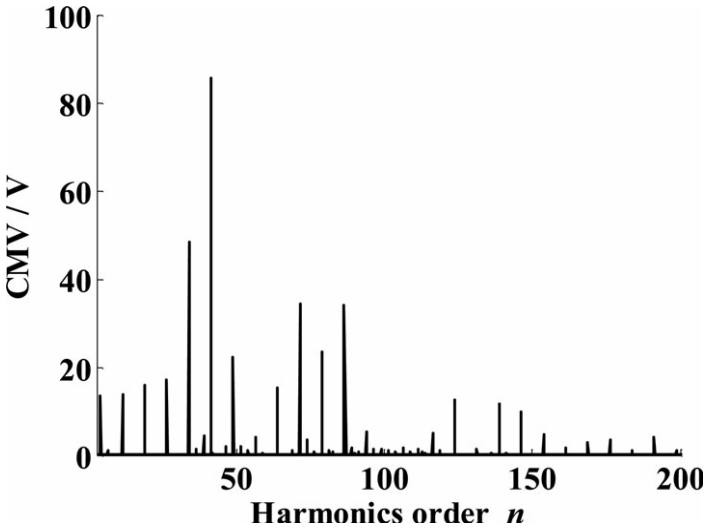

Fig. 7. Spectrum of motor neutral point to dc-link mid-point voltage at 50Hz without passive filter.

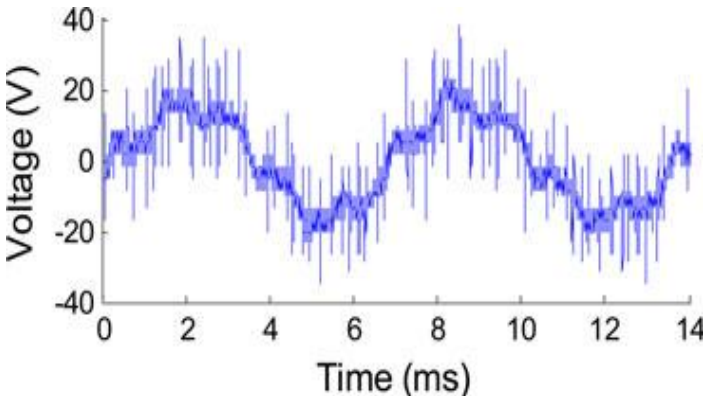

Fig. 8. Waveform of motor neutral point to dc-link mid-point voltage (20V/Div) at 50Hz with passive filter.

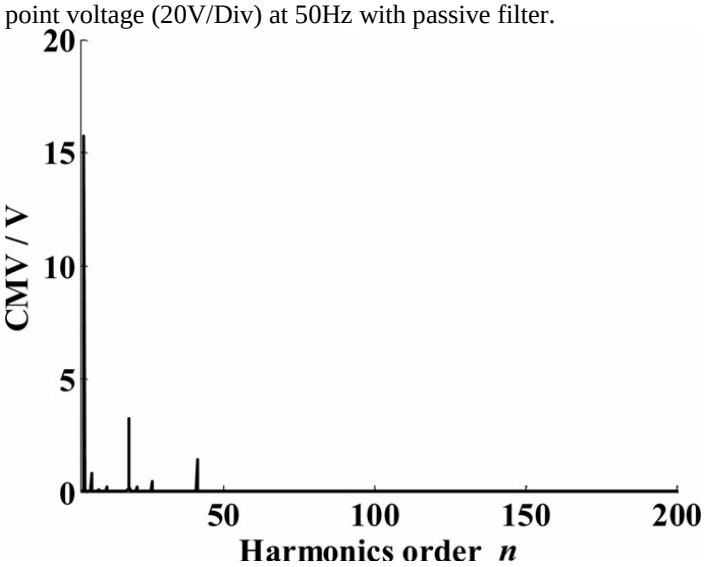

Fig. 9. Spectrum of motor neutral point to dc-link mid-point voltage at 50Hz with passive filter.

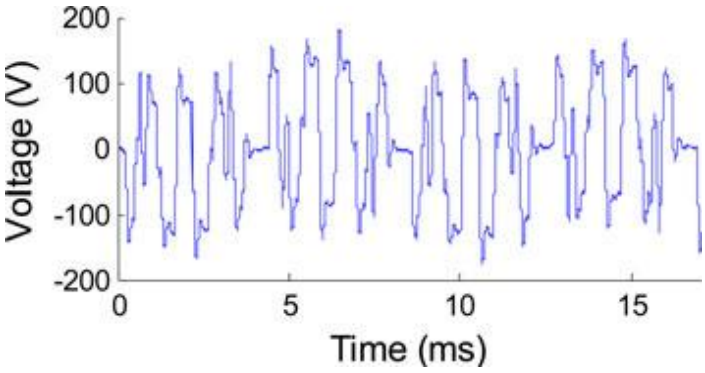

Fig. 10. Waveform of motor neutral point to dc-link mid-point voltage (100 V/Div) at 40 Hz without passive filter.

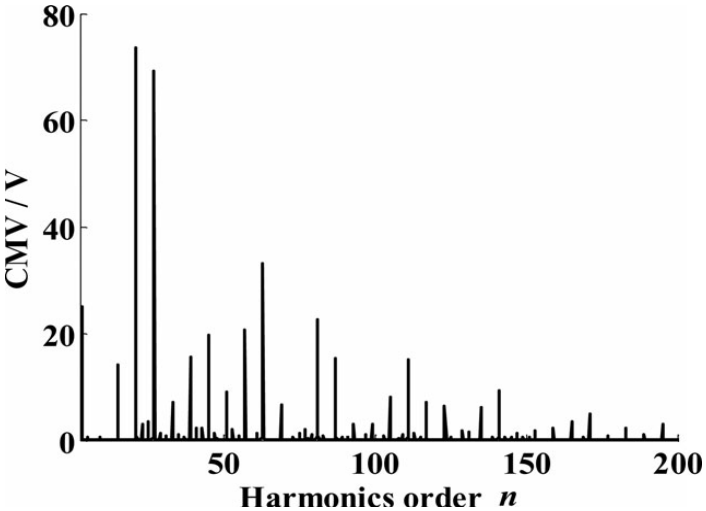

Fig. 11. Spectrum of motor neutral point to dc-link mid-point voltage at 40Hz without passive filter

.

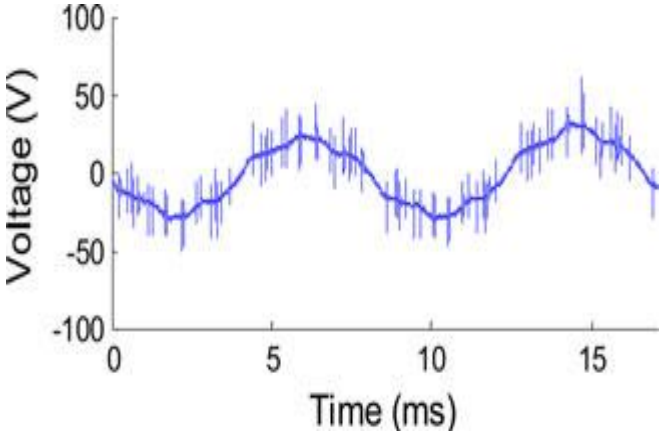

Fig. 12. Waveform of motor neutral point to dc-link mid-point voltage (50V/Div) at 40Hz with passive filter.

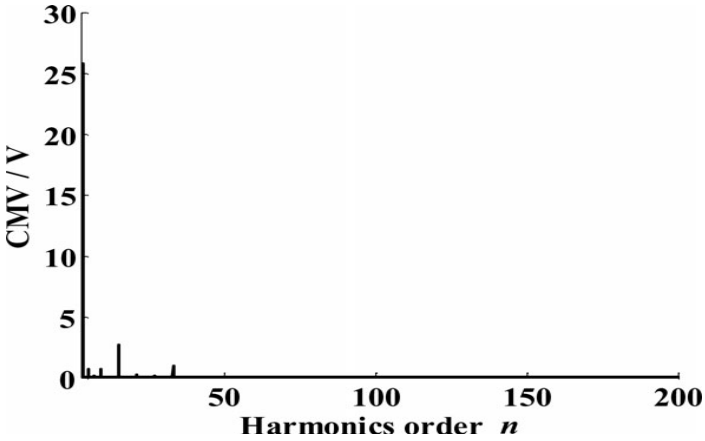

Fig. 13. Spectrum of motor neutral point to dc-link mid-point voltage at 40Hz with passive filter.

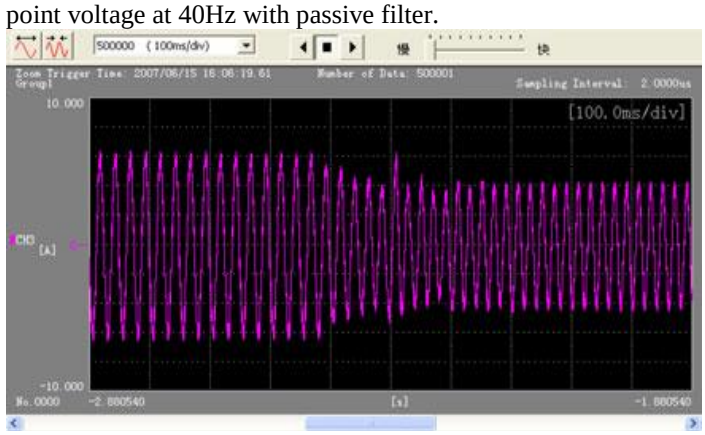

Fig. 14. Motor current when frequency transitioned from 40 to 50Hz(2 A/Div).

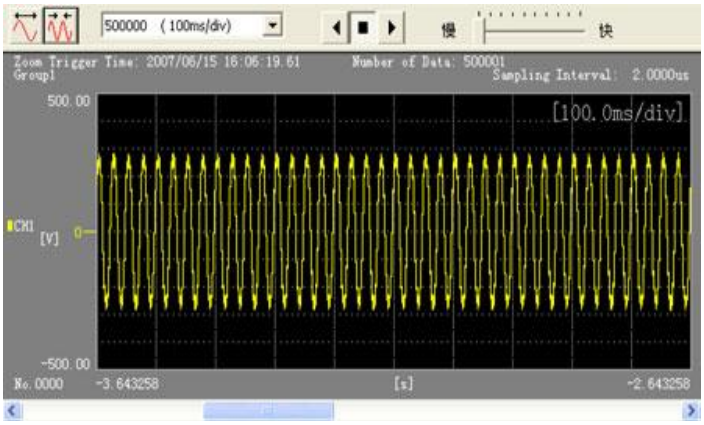

Fig. 15. Motor line voltage when frequency transitioned from 40 to 50Hz (100 V/Div).

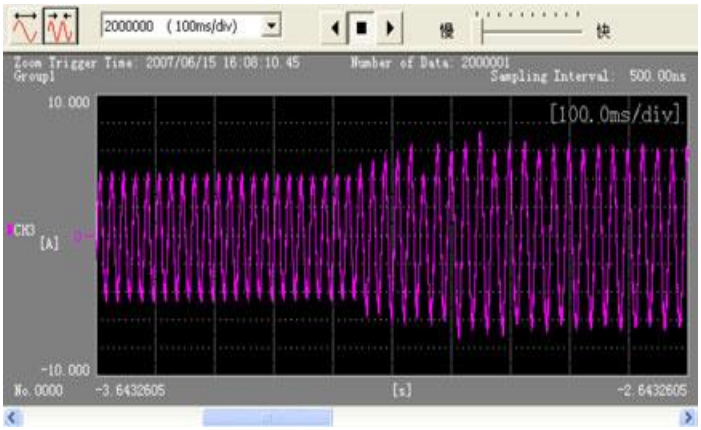

Fig. 16. Motor current when frequency transitioned from 50 to 40Hz (2 A/Div).

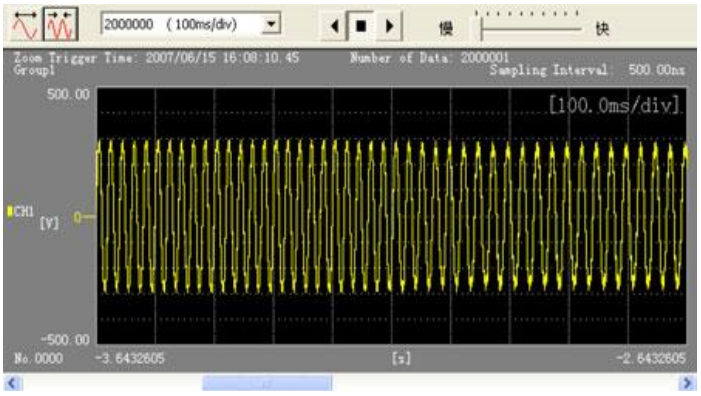

Fig. 17. Motor line voltage when frequency transitioned from 50 to 40Hz (100 V/Div).

at 40 Hz with the passive filter. Comparison of Figs. 10 and 12 shows that the filter was still useful for CMV reduction; however, it was less effective at low frequency; the peak value of the motor neutral point to dc-link mid-point voltage was reduced to 52V from 180V. However, Figs. 12 and 13 show that the motor neutral point to dc-link mid-point voltage was still very small in the drive. This was because the M-SHEPWM scheme could effectively reduce the voltage. This could be seen through comparison of Figs. 6 and 10, which shows that the peak value of the motor neutral point to dc-link mid-point voltage in the C-SHEPWM was 190V, whereas the peak value in the M-SHEPWM was 180V. Comparison of Figs. 7 and 11 also clearly shows that theM-SHEPWMled to reduced motor neutral point to dc-link mid-point voltage; the highest harmonic voltage was 87V in C-SHEPWM and was 73V in M-SHEPWM. Note different scales were used in the aforementioned figures.

The two SHEPWM schemes transitioned at 45 Hz. Figs. 14 and 15 show the motor current and line voltage when the frequency transitioned from 40 to 50 Hz, while Figs. 16 and 17 show the motor current and line voltage when the frequency transitioned from 50 to 40 Hz. These figures clearly show that the two SHEPWM schemes could transition smoothly.

IV SVPWM TECHNIQUE

Space Vector Modulation (SVM) Technique has become the most popular and important PWM technique for three level voltage source inverters for the control of AC Induction Brushless DC,Switched Reluctance and Permanent Manget Synchronous Motors. This work proposes a new soft ware implementation for the three level inverter using Space Vector Modulation technique.Space Vector modulation (SVM) technique was originally developed as a vector approach to pulse-width modulation (PWM) for three-phase inverters. It is a more sophisticated technique for generating sine wave that provides a higher voltage to the motor with lower total harmonic distortion

Space Vector Concept

The concept of space vector is derived from the rotating field of AC machine which is used for modulating the inverter output voltage. In this modulation technique the three phase quantities can be transformed to their equivalent 2-phase quantity either in synchronously rotating frame (or) stationary frame. From this 2-phase component the reference vector magnitude can be found and used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame. Each leg of the DCI can solely take three different switching states. Consequently the DCI has twenty seven valid switching states. Each switching state is denoted with a three letter code (e.g. pnn, pop) which corresponds to the three nodes (a, b, c), respectively, then being connected to the positive (p), zero (o) or negative (n) dc rail. The principle of the SVM is that we use these switching states to compose the desired output voltage. Every switching state corresponds to specific output voltages which are equivalent to a vector on an _-_ plane, using

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \frac{3}{2} & 0 & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

Some switching states are equivalent to the same vector as they match up to the same output voltages. Therefore the switching vectors are only nineteen, as shown in fig. and can be divided into four types: zero vectors (V_0), short vectors (V_1, V2, V_3, V_4, V_5, V_6), medium vectors (V_7, V_6, V_9, V_{10}, V_{11}, V_{12}) and large vectors (V_{13}, V_{14}, V_{15}, V_{16},

V_{17}, V_{18}). The voltages that we want to generate at the output of the inverter can also be matched to a reference vector Vref on an plane using the transformation from equation above.

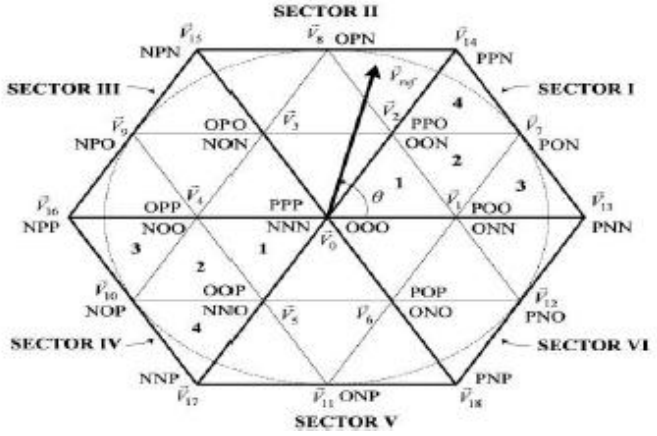

Fig18: Division of sectors and Regions

V SIMULATION RESULTS OF SHEPWM

In this Simulink, the input command frequency is varied fromto 50 hertz and mean while our modulationindex value also varies according to the changes in frequency in such a way that the flux command remains constant. And we observed that the total harmonic distortion is 32.09% and speed is achieved near to synchronous speed.

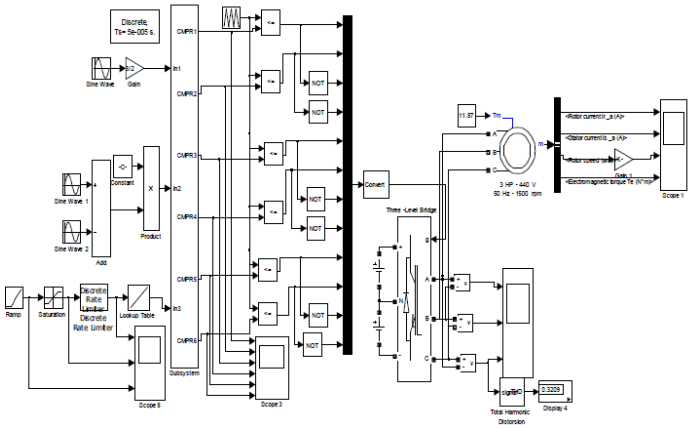

Fig19: Simulink block of Scalar Control

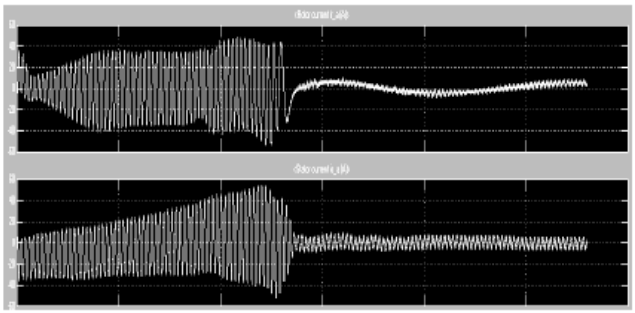

Fig 20: Rotor & Stator currents waveforms

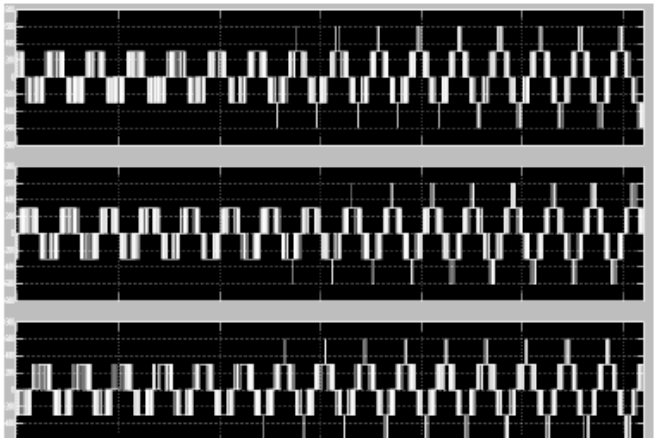

Fig 21: output line-line voltages (V_{ab}.V_{bc},V_{ca})

From this waveform, we observe that it is clearly seen that the wave form changes from two level voltage level to three level as frequency increases from 5 to 50 hertz

VI. CONCLUSION

This paper presents a hybrid SHEPWM scheme to reduce the CMV in a three-level NPC inverter-based induction motor drive for pump and fan applications and Scalar Control Technique in SVPWM Switched Three – Level Inverter Fed Induction Motor The SHEPWM scheme uses the C-SHEPWM to control the inverter at high frequency and the M-SHEPWM at low frequency, to meet the modulation index and CMV requirement of the drive. Experimental results show that the proposed scheme could provide the required modulation index and effectively control the CMV at both low frequency and high frequency. The experimental results also show that the proposed transition scheme could ensure smooth transition between the C-SHEPWM scheme and the M-SHEPWM scheme.

REFERENCES

[1] D. A. Rendusara, E. C. Cengelci, P. N. Enjeti, V. R. Stefanovic, and J. W. Gray, "Analysis of common mode voltage-neutral shift in medium voltage PWM adjustable speed drive (MV-ASD) systems," *IEEE Trans.Power Electron.*, vol. 15, no. 6, pp. 1124–1133, Nov. 2000.

[2] H. Kim, H. Lee, and S. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed AC motor drives," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1840–1845, Nov./Dec. 2001. [3] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters, Principle and Practice*. Hoboken, NJ: Wiley, 2003.

[4] J. Hamman and F. S. Van Der Merwe, "Voltage harmonics generated by voltage-fed inverters using PWM natural sampling," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 297 302, Jul. 1998.

[5] D. Hyypio, "Mitigation of bearing electro-erosion of inverter-fed motors through passive common-mode voltage suppression," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 576–583, Mar./Apr. 2005.

[6] A.V. Jouanne andH. Zhang, "A dual-bridge inverter approach to eliminate common-mode voltage and bearing

and leakage currents," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 43–48, Jan. 1999.
[7] C. Jettanasen, F. Costa, and C. Vollaire, "Common-mode emission measurements and simulation in variable-speed drive systems," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2456–2464, Nov. 2009.
[8] H. Akagi and T. Shimizu, "Attenuation of conducted EMI emissions froman inverter-driven motor," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 282–290, Jan. 2008.
[9] H.Akagi and S. Tamura, "A passive EMI filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1459–1469, Sep. 2006.
[10] H. Akagi and S. Tamura, "A passive filter for an adjustable-speed motor driven by a 400V three-level diode-clamped inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2004, vol. 1, pp. 86–93.
[11] H. Zhang, A. V. Jouanne, S. Dai, A. K.Wallace, and F.Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.
[12] A. Videt, P. Le Moigne, N. Idir, P. Baudesson, and X. Cimetiere, "A
new carrier-based PWM providing common-mode-current reduction and DC-bus balancing for three-level inverters," Dewan, "Generalized techniq
IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 3001–3011, Dec. 2007.
[13] A. Videt, P. Le Moigne, N Idir, P. Baudesson, and J. Ecrabey, "A new carrier-based PWM for the reduction of common mode currents applied to neutral-point-clamped inverters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb./Mar. 2007, pp. 1224–1230.
[14] H. Bierk, N. Benaifa, N. M. Abdel-Latif, and E. Nowicki, "Elimination of low-order harmonics in high power medium voltage inverter applications using a modified SHE-PWM technique," in *Proc. North Am. Power Symp.*,Sep. 2008, pp. 1–4.
[15] W. Fei, Y. Zhang, and X. Ruan, "Solving the SHEPWM nonlinear equations for three-level voltage inverters based on computed initial values," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Feb./Mar. 2007, pp. 1084– 1088.
[16] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel selective harmonic elimination PWMtechniques in series-connected voltage inverters," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 160–170, Jan./Feb. 2000.
[17] A. Maheshwari and K. D. T. Ngo, "Synthesis of six-step pulsewidthmodulated waveforms with selective harmonic elimination," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 554–561, Oct. 1993.
[18] H. R. Karshenas, H. A. Kojori, and S. B.