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Leakage Power Reduction by Using Sleep Methods

Vinay Kumar Madasu[1], B Kedharnath[2]

[1]M. Tech (VLSI), Department of ECE, Gurunanak Institute of Technology[1,]
[2]Professor (HOD), Department of ECE, Gurunanak Institute of Technology[2]
Mail: vinaykumarmadasu3@gmail.com[1], hodece.gnit@gniindia.org[2]

ABSTRACT: In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipation. For the most recent CMOS feature sizes (e.g., 45nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. ITRS reports that leakage power dissipation may come to dominate total power consumption [1]. In the nanometer technology regime, power dissipation and process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power becoming a dominant form of power consumption. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS).This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques at circuit level and process level are used to efficiently minimize leakage current which lead to minimize the power loss and prolong the battery life in idle mode. A novel approach, named "Zigzag keeper," was proposed at circuit level for the reduction of power dissipation. Zigzag keeper incorporate the traditional zigzag approach with keeper which use the sleep transistor plus two additional transistors driven by already calculated output which retain the state of the circuit during the sleep mode while maintaining the state or state retention.

KEYWORDS: Sleep, Dual Sleep, MTCMOS, Low Power Leakage, Forced Stack, Power Dissipation

I. INTRODUCTION:

Power consumption is one of the top issues of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem.

To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area and thus, designers are required to choose appropriate techniques that satisfy application and product needs. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limits the application of each technique. We propose a new approach, thus providing a new choice to low leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper. This paper is organized as follows: Section I give the introduction of different approaches to minimize the power loss. Section II explains the proposed new approach. In section III Simulation and experimental result, we conclude in section IV followed by references.

II PREVIOUS METHODS

This Section reviews the previously proposed approach. In order to compare with the zigzag with keeper approach, this section explains several

previous leakage reduction approaches: sleep, stack, zigzag, dual sleep & dual stack

A. BASE APPROACH

It is a traditional approach. Base approach is generally indicates conventional CMOS transistor. In the base approach pull-up network and pull-down network are used using few transistors. The pull-up network is called a P-MOS transistor and pull-down network is called as N-MOS transistor.

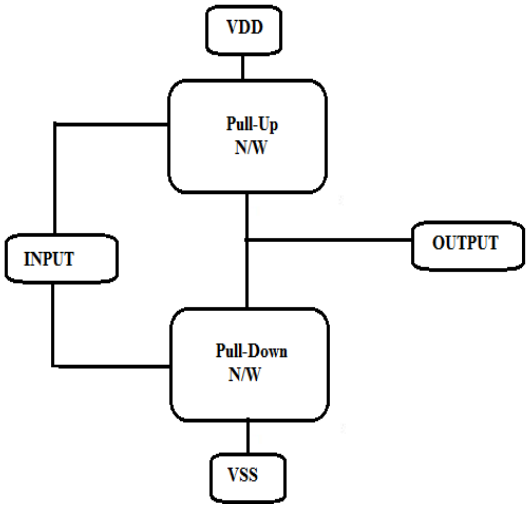

Fig.1: Base Approach

B. SLEEP APPROACH

The most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both(i) an additional "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and Gnd.

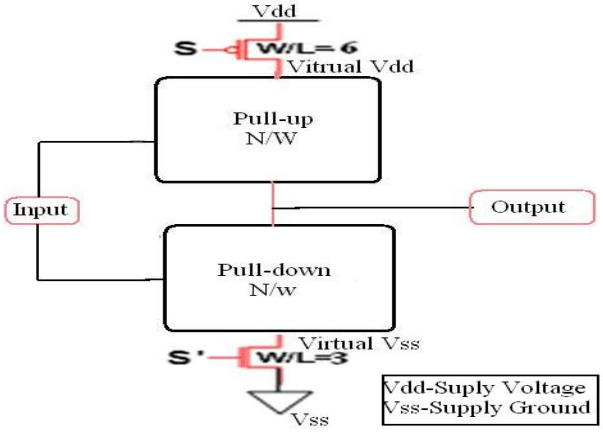

Fig.2: Sleep Approach

C. ZIGZAG APPROACH

The zigzag technique in Figure 3 uses one sleep transistor in each logic stage either in the pull-up or pull-down network according a particular input pattern [4]. Input vector that can achieve the lowest possible leakage power consumption. Then, we either assign a sleep transistor to the pull-down network if the output is „1" or else assign a sleep transistor to the pull-up network if the output is „0." For Figure 3, we assume that the output of the first stage is „1" and the output of the second stage is „0" when minimum leakage inputs are asserted. Therefore, we apply a pull-down sleep transistor for the first stage and a pull-up sleep transistor for the second stage. To reduce the wake-up cost of the sleep transistor technique, the zigzag technique is introduced.

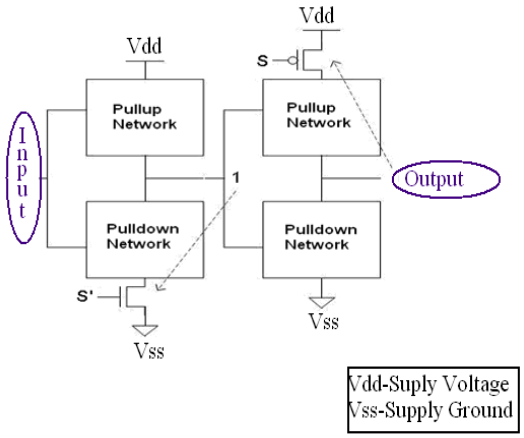

Fig.3: Zigzag Approach

The zigzag technique reduces the wake-up overhead by choosing a particular circuit state (e.g., corresponding to a "reset") and then, for the exact circuit state chosen, turning off the pull-down network for each gate whose output is high while conversely turning off the pull-up network for each gate whose output is low. By applying, prior to going to sleep, the particular input pattern chosen prior to chip fabrication, the zigzag technique can prevent floating

.

D. STACK & SLEEPY STACK APPROACH

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Fig 4 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches.

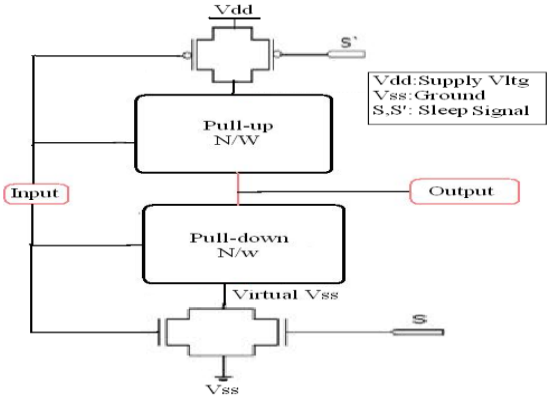

Fig.4: Sleepy Stack Approach

The Sleepy Stack Technique (Fig. 4) combines the Stack & Sleep techniques [2, 3]. The existing transistors divided into two half size transistors in the Sleepy Stack technique like as Stack technique. Between the divide transistors one of sleep transistor will be added in parallel. Stacked transistors suppress leakage current while saving state & Sleep transistors are turned off during sleep mode. In active mode it reduces delay & resistance of the path because of sleep transistor, sleep transistor is placed in parallel to the one of the stacked transistors

E. DUAL SLEEP &DUAL STACK

However, area requirement is max for this technique since every transistor is replaced by three transistors. Dual sleep Technique[8] is (Fig:5) uses the advantage of using the two extra pull- up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply

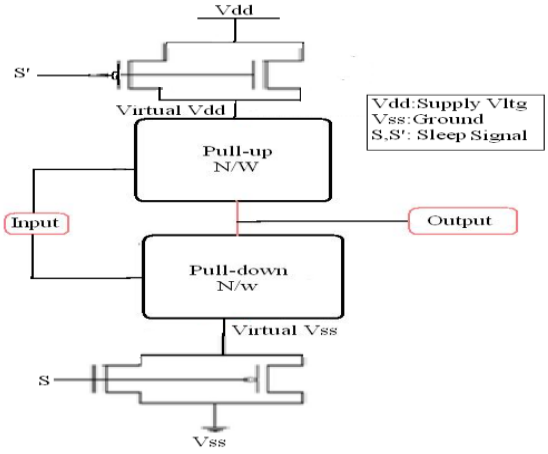

Fig5: Dual Sleep Technique

The method is dual stack approach [1], in sleep mode, the sleep transistors are off, i.e. transistor N1 andP1 are off. We do so by making S=0 and hence S'=1. Now we see that the other 4 transistors P2, P3 and N2, N3 connect the main circuit with power rail. Here we use 2 PMOS in the pull down network and 2 NMOS in the pull-up network. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit.

As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention. Another advantage is got during off mode if we increase the threshold voltage of N2, N3 and P2, P3. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power. If we use minimum size transistors, i.e. aspect ratio of 1, we again get low leakage power due to low leakage current. As a result of stacking, P2 and N2 have less drain voltage. So, the DIBL effect is less for them and they cause high barrier for leakage current. While in active mode i.e. S=1 and S'=0, both the sleep transistors (N1 and P1) and the parallel transistors (N2, N3 and P2, P3) are on. They work as transmission gate and the power connection is again established in uncorrupted way. Further they decrease the dynamic power.

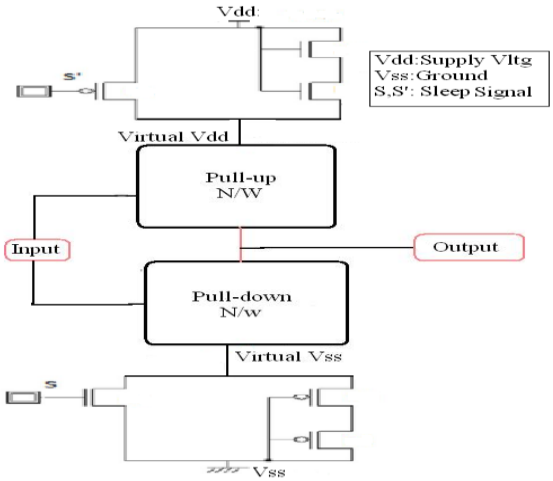

Fig6: Dual Stack Technique

III. PROPOSED METHOD

In the Proposed method there are three modes of operations

(i) In Active mode (AM)
(ii) In Standby mode (SM)
(iii) Sleep to Active mode transition (SAM)

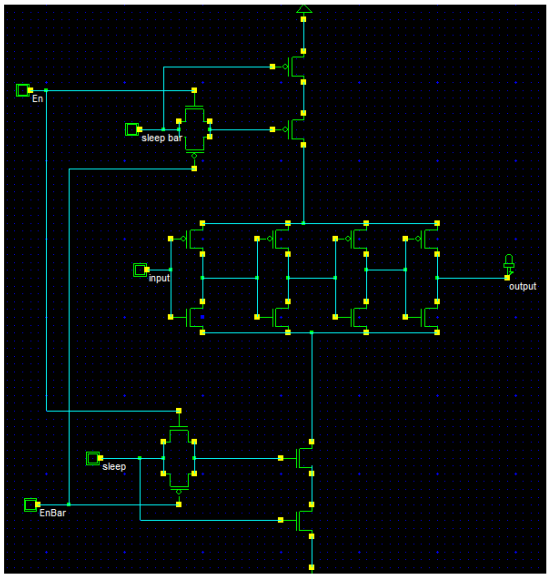

Fig7: Proposed Sleep Method Technique

In AM, both the N2 & P2 sleep transistors remain ON & the sleep Signal (S) of the transistor is held at logic'1' (high). In this case virtual Vss node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the Vdd (supply voltage) & both transistors offer very low resistance. To combining stacked sleep transistors, the magnitude of power supply fluctuations will be reduced because these transitions are gradual during sleep mode transitions, a stacked sleep structures can achieve minimum leakage the with a normal threshold device, while conventional power gating uses a sleep transistor which is a high- threshold device to minimize leakage[2].

In SM, both the T3 & T4 sleep transistors remain ON & the sleep Signal of the transistor is held at logic'1' (high) & control transistors P2 & N2 is OFF by giving logic'0, In this case virtual Vss node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the Vdd (supply voltage) & both transistors offer very low resistance.

By using of the stacking effect we can reduces the leakage current, turning both sleep transistors OFF(T3 & T4) and vice-versa for the header switch.

In SAM, the analyzed design gives major contribution in terms of peak of SM compared to stacking PG. when Sleep mode occurred, the circuit is going from sleep to active or active to sleep. In initial stage, by turning on the control transistor M1 (which is connected across the drain and gate of the T3) then the sleep transistor (T3) is working as a diode.

Due to this Ids of the sleep transistor T3 drops in a quadratic manner. This reduces the circuit wake-up time, voltage fluctuation on the power net & ground. So in SAM, initially after small duration of time we are turning ON transistor T3, to reduce the Ground Bounce Noise T4 will be turned ON. In next stage control transistor is off that sleep transistor works normally. During sleep to active mode transition, transistor T3 & T4 (after a small duration of time) is turned ON. The logic circuit isolated from the ground for a short duration as the transistor T4 is turned OFF.

During this duration, the transistor T4 is operated in triode region, by controlling the intermediate node voltage we can reduce the Ground Bounce Noise & Inserting proper amount of delay (delay < discharging time of the T3transistor). By turning both T3 andT4 sleep transistors OFF, the Leakage current is reduced by the stacking effect. Due to small Id (drain current) it raises the intermediate node voltage VGND2 to +ve values

+ve potential at the intermediate node has 4 effects

- Vgs of T3 becomes negative.
- Negative (body-to-source potential) Vdsl of T3decreases, resulting in less drain induced barrier lowering
- Vds of T4 is less compared to T3, because most of the voltage drops across the T3 in sleep mode.

This significantly reduces the drain barrier lowering. Hence the reduction of leakage power is done in circuit [7].

IV. SIMULATION RESULT

Fig7 & Fig8 show the logic and power consumption, respectively for an NAND. For circuit design & circuit logic verification we use DSCH (Digital schematic), for CMOS layout verification & power calculation of the circuit we use MWND(Microwind) Fig7 & Fig8 show the logic and power consumption, respectively for a chain of 4 inveters

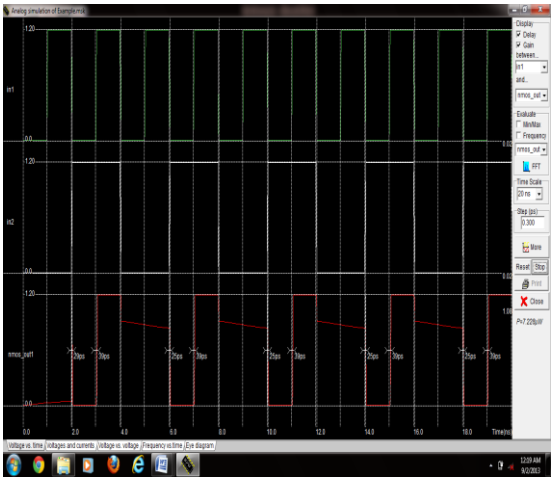

Fig8: Power consumption of proposed sleep method

Logic Circuit	Power Consumption
Basic Chain of 4 Inverters	13.088µw
Sleepy Chain of 4 Inverters	7.228µw
With Proposed Sleep Method	3.121µw

Table 1: Comparison b/w Proposed method with other techniques

V.CONCLUSION

Sub threshold leakage power consumption is a great challenge in nano-meter scale (CMOS) technology, although previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, based upon technology & design criteria the designers can choose the techniques. In this paper, we provide novel circuit structure in terms of static & dynamic powers named as "Power gated sleep method" it's a new remedy for designers. This technique shows the least speed power product among all techniques. The Proposed technique achieving ultra-low leakage power consumption with much less speed, especially it shows nearly 50-60% of power than the existing. So, it can be used for future IC'S for area & power Efficiency

VI.REFERENCES

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VII.BIOGRAPHY:

Vinay Kumar Madasu did his B.Tech in ECE from Vivekananda Institute of Technology (JNTUH) and persuing the M.Tech in VLSI-SD from Gurunanak Institute of Technology, Hyderabad in 2013. His areas of interest in research are Low power Design & Analog Designs

Mr.B.Kedharnath did his M.Tech from Institute Advance studies for Education, India and persuing Ph.D from Rayalaseema University. He is working as Head of the Department, Professor in the

department of Electronics & Communication Engineering, Gurunanak Institute of Technology, Hyderabad, India. His areas of interest in research are Microwave, Radar & Wireless communications