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Performance Evaluation of Low Power Dynamic Circuit Using Footed Diode Domino Logic

Monika Jain[1], Dr. Subodh Wairya[2]

[1] Electronics Engineering Department, Institute of Engineering & Technology,
Gautam Buddh Technical University,
Lucknow-226021, U.P, India
2507monika@gmail.com

[2]Associate Professor
Electronics Engineering Department, Institute of Engineering & Technology,
Gautam Buddh Technical University,
Lucknow-226021, U.P, India
swairya@ietlucknow.edu

Abstract: ***Power saving is more important than any other thing now a days because high speed and low power design continues to get more attention. In this paper, low power dynamic circuit [1] has been implemented at 180nm, 90nm, 45nm and 32nm technology, using HSPICE. The simulations are performed on CosmosScope. The power saved is up to 46%, 50%, 51% and 73% for 180nm, 90nm, 45nm and 32nm technology respectively using the proposed footed diode circuit [1]. Domino buffer and a two input AND gate have been used as a test circuit to show the simulation results.***

Keywords: Domino logic, power consumption, PDB based domino logic, footed diode.

1. Introduction

Domino logic is one of the dynamic logic circuits followed by a static CMOS inverter . The operation of this circuit is controlled by a clock signal. The parasitic capacitance, located just before the static inverter, stores the output voltage and passes it to the next stage. The domino logic circuit works in two phases. They are precharge phase and evaluation phase.

1.1 Precharge phase

When the clock is low, it is called the precharge phase. In this phase, the output node of the dynamic CMOS stage is precharged to a high logic level, and the output of the CMOS inverter (buffer) becomes low.

1.2 Evaluation phase

When the clock is high, it is called the evaluation phase. At the beginning of the evaluation phase, when the clock signal rises, there are two possibilities : The output of the dynamic CMOS stage is either discharged to a low level through the NMOS circuitry(1 to 0 transition), or it could remain high. As a result, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1, irrespective of the value of the inputs applied to the dynamic CMOS stage. Because of transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase.

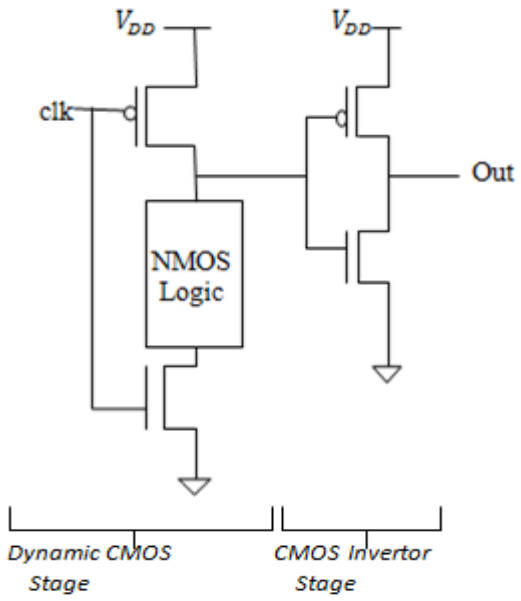

Figure 1: Generalized circuit diagram of a domino CMOS logic gate

An extra noise is introduced to the dynamic circuit in precharge phase. To avoid this noise TSPC based dynamic logic circuit is used. The drawback being that an extra clock transistor is used in output stage static inverter. However, while using TSPC based dynamic logic circuit, performance

degradation is monitored in the circuit due to the propagation of precharge pulse from dynamic node to the output node. This problem can be compensated through PDB based domino logic.

2. PDB Based Domino Buffer

In pseudo dynamic buffer, the NMOS transistor M5 of the static inverter, used in conventional domino buffer, is connected to node X instead of ground (as shown in figure 2). As a result, during the precharge phase when clock pulse is low, the value of dynamic node Y cannot propagate to the output node because of the disabled NMOS clock transistor M2.

When input A is low, dynamic node Y is always high and output is low irrespective operating phase.

When input A is made high, the circuit will efficiently operated under two phases namely precharge phase and evaluation phase [2].

2.1 Evaluation phase

In this phase, when clock pulse is high, the PMOS transistor Ml is turned off and NMOS transistor turned on. As a result the dynamic node Y discharges through node X and makes the output node high.

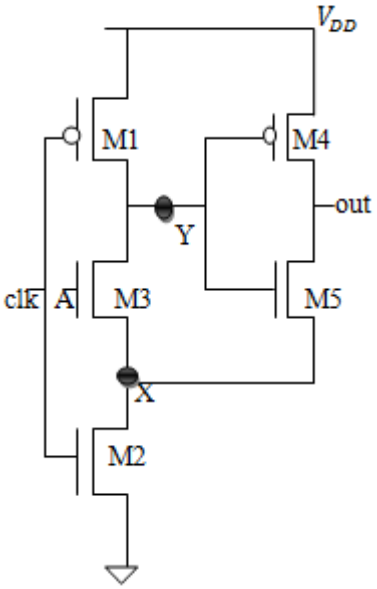

Figure 2: Domino buffer using pseudo dynamic buffer

2.2 Precharge phase

When clock pulse is kept low, transistor M1 is turned on and M2 is turned off. As a result, the PMOS transistor M5 is turned on and dynamic node Y gets charged to V_{DD}. The output is still high because the clock pulse turns off the transistor M2, which does not allow the output node to discharge.

3. Footed Diode Based Domino Buffer

The performance degradation monitored in the TSPC based dynamic buffer was compensated by PDB based design for domino logic, but only up to some extent. It can still be improved by a footed diode based domino logic[1].This circuit will reduce the power consumption up to 90% while using different technologies as compared to conventional domino buffer.

3.1 Footed diode based domino buffer

In this circuit, an extra NMOS transistor M6 is being used as a diode in between ground and clock transistor M2. Let us take an example of a diode footed buffer shown in the figure 3. We can see that the source of the NMOS transistor M5 is connected to the node X instead of the ground.

When input A is low, the dynamic node Y is always high and output is kept low regardless of operating phase and when the input A is high, circuit will operate under two phases namely precharge and evaluation phase [2].

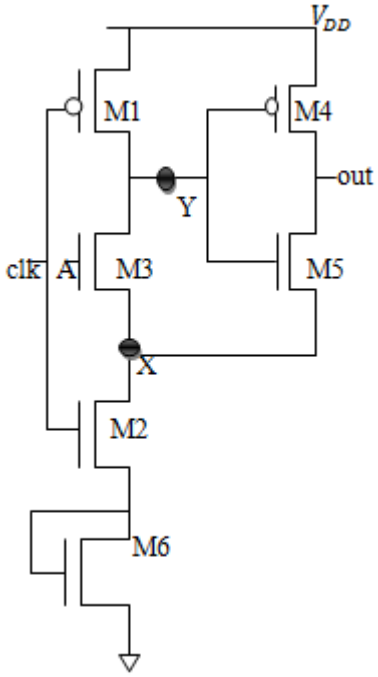

Figure 3: Domino logic buffer using footed diode

3.1.1 Evaluation phase

When the clock pulse is high, the PMOS transistor M1 is turned off and NMOS transistor M2 is turned on. As a result, the dynamic node Y discharges through node X and the output node becomes high.

3.1.2 Precharge phase

When clock pulse is low then PMOS clock transistor M5 is turned on and dynamic node Y is charged to V_{DD}. The output is still high as the transistor M2 is turned off by the clock pulse. So, M6 is also off and thus the output node is not able to discharge. Due to stacking effect power is compensated.

3.2 Footed diode based 2-input domino AND gate

A Footed diode based 2-input domino AND gate is shown in figure 4. The inputs to the gate are A and B with the footed NMOS transistor M7.The working is same as the footed diode domino buffer. This circuit can also work in two phases, namely, precharge phase and evaluation phase. In precharge phase, the clock signal is low (clk=0) and in evaluation phase, the clock signal is high (clk=1).

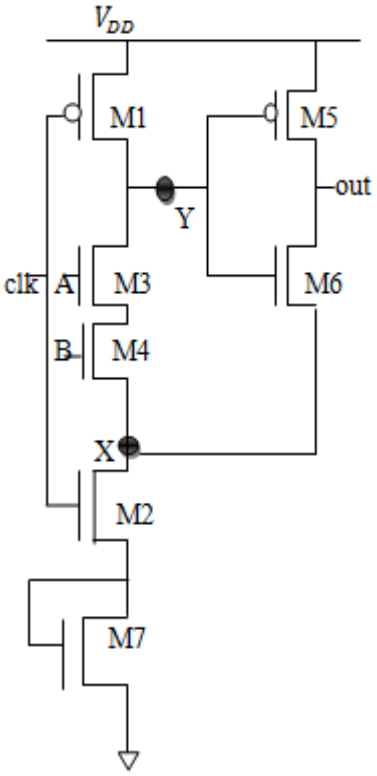

Figure 4: 2-input domino logic AND gate using footed diode

4. Simulation Results

To evaluate the performance of the PDB based domino logic and the footed diode technique [1], we have used 180nm, 90nm, 45nm and 32nm standard CMOS technologies. In order to show the power saving of our techniques, simulation was performed using CosmosScope and the coding was done on HSPICE.

The simulation results for the power dissipation in buffer using different technologies is shown in Table-1, and the percentage of power saved by each technique is shown in Table-2.

TABLE 1. Power dissipation in domino buffer using different logics at different CMOS technologies.

	Power (Conventional) (uW)	*Power (TSPC) (uW)*	*Power (PDB) (uW)*	*Power (Footed Diode) (uW)*
180nm	9.51	8.83	6.415	5.876
90nm	2.04	2.016	1.513	1.292
45nm	5.767	4.548	3.576	2.721
32nm	0.3026	0.2923	0.2270	0.1694

TABLE 2. Percentage of power saved in domino buffer using different logics at different CMOS technologies

	Power Saved (TSPC)In%	*Power saved (PDB)in%*	*Power saved (Footed Diode)In %*
180nm	7.1	32.5	39
90nm	1.1	25.83	36.66
45nm	21.13	37.99	52.81
32nm	3.40	24.98	44.01

The simulation results for the power dissipation in 2-input AND gate using different technologies is shown in Table-3, and the percentage of power saved by each technique is shown in Table-4.

TABLE 3. Power dissipation in 2-input domino AND using different logics at different CMOS technologies.

	Power (Conventional)(uW)	*Power (TSPC) (uW)*	*Power (PDB) (uW)*	*Power (Footed Diode)(uW)*
180nm	12.02	11.25	8.7	6.463
90nm	3.055	2.695	2.119	1.504
45nm	6.534	5.263	4.451	3.162
32nm	0.7571	0.4211	0.3703	0.1993

TABLE 4. Percentage of power saved in 2-input domino AND using different logics at different CMOS technologies.

	Power Saved (TSPC)In %	*Power saved (PDB) In %*	*Power saved (Footed Diode) In %*
180nm	6.4	27	46.7
90nm	11.81	30.63	50.76
45nm	19.45	31.87	51.60
32nm	4.43	51.08	73.67

5. Conclusion

This paper shows the simulation results of a buffer and a 2-input AND gate implemented using PDB based domino logic and footed diode domino logic style [1]. The coding and simulations are done on HSpice and CosmosScope, respectively at 180nm, 90nm, 45nm and 32nm technologies. The simulation result shows that compared to the conventional logic the power is saved up to 36%, 30%, 37% and 51% for 180nm, 90nm, 45nm and 32nm technology respectively when PDB based logic style is used and up to 46%, 50%, 51% and 73% for 180nm, 90nm, 45nm and 32nm technology respectively when footed diode based logic style is used.

References

[1] "Design and Simulation of Low Power Dynamic Logic Circuit Using Footed Diode Domino Logic" by Sujeet Kumar, Sanchit Singhal, Amit Kumar Pandey and R K Nagaria

[2] Tyler Thorp, Dean Liu, Pradeep Trivedi, Analysis of blocking dynamic circuits, IEEE Transactions on VLSI Systems (2003), pp. 744-749

[3] Brief Introduction to HSPICE Simulation, by Wojciech Giziewicz.

[4] CMOS Digital Integrated Circuits, Analysis and Design, by Sung-Mo (Steve) Kang and Yusuf Leblebigi.

[5] Digital Circuit Simulation Using HSPICE, by Charles R. Kime.

[6] Neil H.E. Weste, David Harris, Principles of CMOS VLSI Design: A System Perspective, (3rd ed.) Addison-Wesley (2004).

[7] Y. Ji-Ren, I. Karlsson, C. Svensson, A true single-phase-clock dynamic CMOS circuit technique, lEEE Journal of Solid-State Circuits, 22 (Oct.) (1987), pp. 899-90I.

[8] Fang Tang, Amine Bermark, Zhouye Gu, "Low power dynamic logic design using a pseudo dynamic buffer, INTEGRATION", the vlsi journal 45(2012) 395-404.

Author Profile

Monika Jain received the B. Tech degree in Electronics and Communication Engineering from Priyadarshini College of Computer sciences, Uttar Pradesh Technology University, Greater Noida, India and is currently working towards her M. Tech degree in Microelectronics with the research interest in Reducing power consumption and leakage currents in digital circuits, form Institute of Engineering and Technology, Uttar Pradesh Technology University, Lucknow, India.

Dr. Subodh Wairya received B. Tech (1993), M.Tech and Ph.D (2012) from HBTI, Kanpur, Jadavpur University, Kolkata and MNNIT Allahbad, India, respectively. His Ph.D research work was oriented towards PERFORMANCE EVALUATION OF HIGH SPEED LOW POWER CMOS FULL ADDER CIRCUITS FOR LOW VOLTAGE VLSI DESIGN. Currently, he is an Associate Professor at IET, lucknow(from 6 May 1996- Present).He has also served as Scientist "B" Adhoc (One Year) at DRDO, Lucknow during January, 1995-January, 1996 and Graduate Engineer under Consultancy Project at HAL, Lucknow during From January, 1994-January, 1995 (one year). Also he is one of the authors of a book entitled "A Simplified Approach to Telecommunication and Electronic Switching Systems" by C.B.L. Srivastav, Neelam Srivastava & Subodh Wairya Published by Dhanpat Rai and Company in the year 2006.