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FPGA Based Low Area Motion Estimation with BISCD Architecture

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Abstract: *The Motion Estimation Computing Array (MECA) is used in Video Encoding applications to calculate the best motion between the current frame and reference frames. The MECA is in decoding application occupies large amount of area and timing penalty. By introducing the concept of Built-in Self test technique the area overhead is increased in less amount of area. In this Paper the Built-in Self test Technique (BIST) is included in the MECA and in each of Processing Element in MECA is tested using residue codes .the quotient and remainder was cross checked across the processing element and test code generator. Further the residue and quotient code complex operation is replaced with the simple Boolean logic division operation in order to reduce the area of the circuit. Thus by introducing the BIST Concept the testing is done internally without Connecting outside testing Requirements. So the area required is also reduces. And in this Paper the Errors in MECA are Calculated and the Concept of Diagnoses i.e. Self Detect and Self Repair Concepts are introduced.*

Keywords: Build in Self Detection and Correction (BISDC), Area Overhead, Time penalty, Data recovery, Error detection, Motion Estimation, Processing Element (PE), Residue-and-Quotient (RQ) code,

1. Introduction

In more recent years, multimedia technology applications have been becoming more flexible and powerful with the development of semiconductor technology. The latest video standard, H.264/AVD/MPEG_4 part 10 (Advance Video Coding) is regarded as the next generation video compression standard (VCS). For video compression standards, the motion estimation computing array (MECA) is the most computationally demanding component in a video encoder/decoder where about 60-90% of the total of computation time is consumed in motion estimation. Generally, motion estimation computing array (MECA) performs up to 50% of computations in the entire video coding system. Thus, integrating the MECA into a system-on-chip (SOC) design has become increasingly important for video coding applications [1].

Although advances in VLSI technology allow integration of a large number of processing elements (PEs) in an MECA [2]-[4] into an SOC, this increases the logic-per-pin ratio, thereby significantly decreasing the efficiency of chip logic testing. For a commercial chip, a video coding system must introduce design for testability (DFT), especially in an MECA.

The objective of DFT is to increase the ease with which a device can be tested to guarantee high system reliability. Many DFT approaches have been developed. These approaches can be divided into three categories: ad hoc (problem oriented), structured, and built-in self-test (BIST). Among these techniques, BIST has an obvious advantage in that expensive test equipment is not needed and tests are low cost.

This project develops a built-in self-detection and correction (BISDC) architecture for motion estimation computing arrays(MECAs).Based on the error detection & correction concepts of bi residue codes, any single error in each processing element in an MECA can be effectively detected and corrected online using the proposed BISD and built-in self-correction circuits. Performance analysis and evaluation demonstrate that the proposed BISDC architecture performs well in error detection and correction with minor area.

The Motion Estimation Computing Array is used in Video Encoding applications to calculate the best motion between the current frame and reference frames. The MECA is in decoding application occupies large amount of area and timing penalty. By introducing the concept of Built-in Self test technique the area overhead is increased in less amount of area. In this Paper the Built-in Self test Technique (BIST) [5] is included in the MECA and in each of Processing Element in MECA. Thus by introducing the BIST Concept the testing is done internally without Connecting outside testing Requirements. So the area required is also reduces. And in this Project the Errors in MECA are Calculated and the Concept of Diagnoses i.e. Self Detect and Self Repair Concepts are introduced. The area results are compared with the MECA without BIST technique.

2. RQ CODE

Coding approaches such as parity code, Berger code [7], and residue code have been considered for design applications to detect circuit errors. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented.

However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. There-fore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors.

3. Proposed Architecture Design

3.1. Conceptual view of the proposed BISDC architecture:

Fig.1 shows the conceptual view of the proposed BISDC scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in Fig. 3 utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery.

In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG.

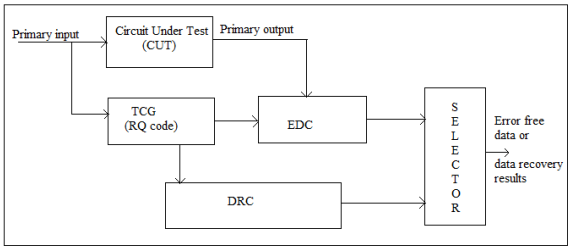

Fig.1.Conceptual view of the proposed BISDC architecture

Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array based computing structure, such as ME[10], discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed BISDC scheme to detect errors and recover the corresponding data

This work adopts the systolic ME as a CUT to demonstrate the feasibility of the proposed BISDC architecture. A ME consists of many PEs in order to determine the sum of absolute difference (SAD) value for video encoding [8] applications and some registers and latches may exist in ME to complete the data shift and storage.

3.2. A Specific PEi testing processes of the proposed BISDC architecture:

Fig.2 shows the proposed BISDC circuit design for a specific PE_i of a ME. The self-detection and self correction operations (Fig.1) are simply described as follows. First, the input data of cur_ Pixel and Ref_pixel for a specific PE_i in the MECA are sent to the test code generator (TCG) to generate the corresponding test codes.

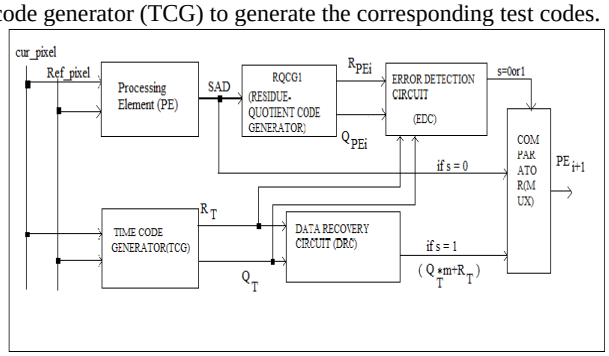

Fig.2.A Specific PE_i testing processes of the proposed BISDC architecture

Second, the test codes from the TCG and output data from the specific PE_i are detected and verified in Error Detection Circuit (EDC) to determine whether the specific PE_i has an error. In other words, the self-detection capability uses the detect the error. Third, the Data recovery circuit (DRC) comes to play for error correction. Finally, the error correction data from DRC, or error-free data from the EDC, are passed to the next specific PE_{i+1} for subsequent testing.

3.3. TEST CODE GENERATOR:

TCG is an important component of the proposed BISDC architecture. Notably, TCG design is based on the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data. The specific in Fig. 2.estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macro block. Thus, by utilizing PEs[6], SAD shown in as follows, in a macro block with size of N × N can be evaluat ed

$$SAD = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} |X_{ij} - Y_{ij}|$$
$$= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} \left|(q_{xij}\cdot m + r_{xij}) - (q_{yij}\cdot m + r_{yij})\right| \quad \text{----(1)}$$

Where and denote the corresponding RQ code of and modulo. Importantly, and represent the luminance pixel value of Cur_pixel and Ref_pixel, respectively. Based on the residue code, the division operation can be applied to facilitate generation of the RQ code (and) form TCG. Namely, the circuit design of TCG can be easily achieved (see Fig. 3 by using equations (2) & (3) we use to derive corresponding RQ code.

The remainder is computed as follows

$$\begin{aligned} R_T &= \left|\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij} - Y_{ij})\right|_m \\ &= \left|\left|(X_{00} - Y_{00})\right|_m + \left|(X_{01} - Y_{01})\right|_m + \cdots \right. \\ &\quad \left. + \left|\left(X_{(N-1)(N-1)} - Y_{(N-1)(N-1)}\right)\right|_m\right|_m \\ &= \left|\left|(q_{x00}\cdot m + r_{x00}) - (q_{y00}\cdot m + r_{y00})\right|_m \right. \\ &\quad + \cdots \left|\left(q_{x(N-1)(N-1)}\cdot m + r_{x(N-1)(N-1)}\right)\right. \\ &\quad \left.\left. - \left(q_{y(N-1)(N-1)}\cdot m + r_{y(N-1)(N-1)}\right)\right|_m\right|_m \\ &= \left|\left|(r_{x00} - r_{y00})\right|_m + \left|(r_{x01} - r_{y01})\right|_m + \cdots \right. \\ &\quad \left. + \left|\left(r_{x(N-1)(N-1)} - r_{y(N-1)(N-1)}\right)\right|_m\right|_m \\ &= \left|\left|r_{00}\right|_m + \left|r_{01}\right|_m + \ldots + \left|r_{(N-1)(N-1)}\right|_m\right|_m \quad \text{-----(2)} \end{aligned}$$

The quotient is computed as follows

$$Q_T = \left\lfloor \frac{\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij}-Y_{ij})}{m} \right\rfloor$$
$$= \left\lfloor \frac{(X_{00}-Y_{00})+(X_{01}-Y_{01})+\ldots+(X_{(N-1)(N-1)}-Y_{(N-1)(N-1)})}{m} \right\rfloor$$
$$= \left\lfloor \frac{(q_{x00}\cdot m - q_{y00}\cdot m)}{m} + \frac{(r_{x00}-r_{y00})}{m} + \frac{(q_{x01}\cdot m - q_{y01}\cdot m)}{m} + \frac{(r_{x01}-r_{y01})}{m} + \ldots \right\rfloor$$
$$= \left\lfloor \frac{(q_{x00}-q_{y00})+(q_{x01}-q_{y01})+\ldots+\frac{(r_{x00}-r_{y00})+(r_{x01}-r_{y01})+\ldots}{m} \right\rfloor$$
$$= q_{00}+q_{01}+\ldots+q_{(N-1)(N-1)} + \left\lfloor \frac{(r_{00}+r_{01}+\ldots+r_{(N-1)(N-1)})}{m} \right\rfloor \quad \text{-------(3)}$$

Under the faulty case, the RQ code from $RQCG_2$ of the TCG is still equal to (2) and (3). However, R_{PEi} and Q_{PEi} are changed to (13) because an error e has occurred. Thus, the error in a specific PE_i can be detected if and only if (2) ≠ (4) and/or (3) ≠ (5).

$$R_{PE_i} = |SAD'|_m = \left| \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij}-Y_{ij})+e \right|_m$$
$$= |r_{00}{}_m + |r_{01}{}_m + \ldots + r_{(N-1)(N-1)}{}_m + |r_e{}_m|_m \quad \text{-----(4)}$$
$$Q_{PE_i} = \left\lfloor \frac{SAD'}{m} \right\rfloor = \left\lfloor \frac{\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij}-Y_{ij})+e}{m} \right\rfloor$$
$$= q_{00}+q_{01}+\ldots+q_{(N-1)(N-1)}+q_e + \left\lfloor \frac{(r_{00}+r_{01}+\ldots+r_{(N-1)(N-1)})+r_e}{m} \right\rfloor . \quad \text{-----(5)}$$

During data recovery, the circuit DRC plays a significant role in recovering RQ code from TCG. The data can be recovered by implementing the mathematical model as

$$SAD = m \times Q_T + R_T$$
$$= (2^j - 1) \times Q_T + R_T$$
$$= 2^j \times Q_T - Q_T + R_T, \quad \text{-----(6)}$$

To realize the operation of data recovery in (6), a Barrel shift [23] and a corrector circuits are necessary to achieve the functions of (2^j X Q_T) and ($-Q_T + R_T$), respectively. Notably, the proposed BISDC design executes the error detection and data recovery operations simultaneously.

Additionally, error-free data from the tested PE_i or the data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific PE_{i+1} for subsequent testing.

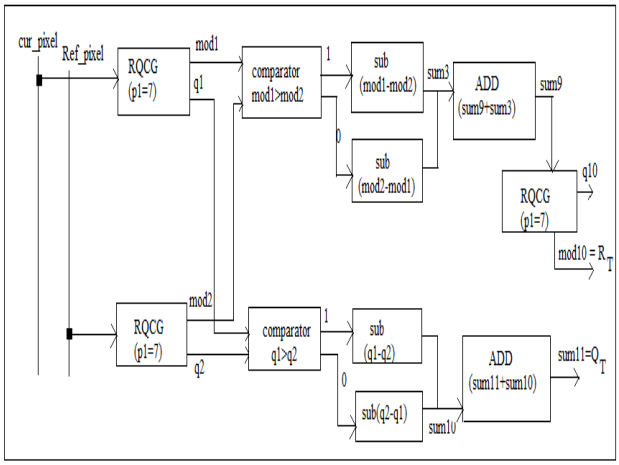

Fig.3. Circuit design of the TCG

4. OVERALL TEST STRATERGY

By extending the testing processes of a specific PE_i in Fig. 2, Fig. 4 illustrates the overall BISDC architecture design of a ME. First, the input data of Cur_pixel and Ref_pixel are sent simultaneously to PEs and TCGs in order to estimate the SAD values and Design of An Error generate the test RQ code R_T and Q_T. Second, the SAD value from the tested object PE_i, which is selected by MUX_1, is then sent to the RQCG circuit in order to generate R_{PEi} and Q_{PEi} codes.

Meanwhile, the corresponding test codes R_{Ti} and Q_{Ti} from a specific TCG_i are selected simultaneously by MUXs 2 and 3, respectively. Third, the RQ code from TCG_i and RQCG circuits are compared in EDC to determine whether the tested object PE_i have errors.

The tested object PE_i is error-free if and only if $R_{PEi} = R_{Ti}$ and $Q_{PEi} = Q_{Ti}$. Additionally, DRC is used to recover data encoded by TCG_i, i.e. the appropriate R_{Ti} and Q_{Ti} codes from TCG_i are selected by MUXs 2 and 3, respectively, to recover data. Fourth, the error-free data or data recovery results are selected by MUX_4. Notably, control signal S_4 is generated from EDC, indicating that the comparison result is error-free ($S_4 = 0$) or errancy ($S_4 = 1$).

Finally, the error-free data or the data-recovery result from the tested object PE_i is passed to a De-MUX, which is used to test the next specific PE_{i+1}; otherwise, the final result is exported.

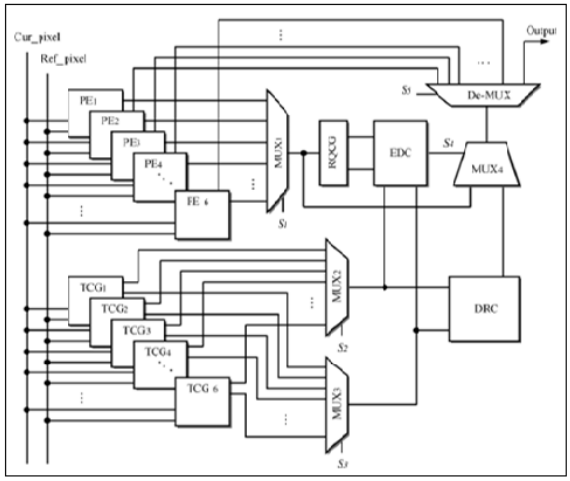

Fig .4. Proposed BISDC architecture design for a ME.

5. RESULTS AND DISCUSSION

Extensive verification of the circuit design is performed using the VHDL, executed on Windows 7 operating system and synthesized using Xilinx ISE simulator on XC3S100E device to demonstrate the feasibility of the proposed BISDC architecture design for ME testing applications.

5.1. Experimental Results

Table.1.summarizes the synthesis results of area overhead and time penalty of the proposed BISDC architecture. The area is estimated based on the number of gate counts. By considering 16 PEs in a ME and 16 TCGs of the proposed BISDC architecture, the area overhead of error detection, data recovery, and overall BISDC architecture (AO_{ED} , AO_{DR}, and AO_{EDDR}) are

$$AO_{ED} = \frac{(759+2120\times16+63)}{(348\times16)} = 6.239$$

$$AO_{DR} = \frac{(2120\times16+389)}{(348\times16)} = 6.1618$$

$$AO_{BISDC} = \frac{(759+63+2120\times16+389)}{(348\times16)} = 6.309$$

Components	PE	RQCG	EDC	TCG	DRC
Area (Gate counts)	348	759	63	2120	389
Operation Time (ns)	27.991	25.461	7.043	39.700	13.222
Area Overhead			6.309		
Time Penalty			0.891		

Table.1.Estimation of area overhead and time penalty

The time penalty is another criterion to verify the feasibility of the proposed BISDC architecture. Table I also summarizes the operating time evaluation of a specific and each component in the proposed BISDC architecture. The following equations show the time penalty of error detection and data recovery

(TP_{ED} and TP_{DR}) operations for a 4× 4 macro block (a PE_i With 16 pixels):

$$TP_{ED} = \frac{((39.700+7.043)-27.991)}{(27.991)} = 0.669$$

$$TP_{DR} = \frac{((39.700+13.222)-27.991)}{(27.991)} = 0.891$$

Notably, each PE of a ME is tested sequentially in the proposed BISDC architecture. Thus, if the proposed BISDC architecture is embedded into a ME for testing, in which the entire timing penalty is equivalent to that for testing a single PE., i.e. approximately about 0.669and 0.891 time penalty of the operations of error detection and data recovery, respectively. The operating time of the RQCG circuit can be neglected to evaluate because TCG covers the operating time of RQCG. Additionally, the error-free/errancy signal from EDC is generated after 46.743 ns (39.700+7.043). Thus, the error-free data is selected directly from the tested object because the operating time of the tested object is faster than the results of data recovery from DRC.

5.2. Performance Discussion:

The TCG component plays a major role in the proposed BISDC architecture to detect errors and recover data. Additionally, the number of TCGs significantly influences the circuit performance in terms of area overhead. Figs. 5 illustrate the relations between the TCG and Area overhead. TCGs, area overhead and throughput. The area overhead is less than 0.22if only one TCG is used to execute; although the area overhead is increases if 16 TCGs used (see Fig. 5), the area overhead is only about 6.309, i.e. an acceptable design for circuit testing.

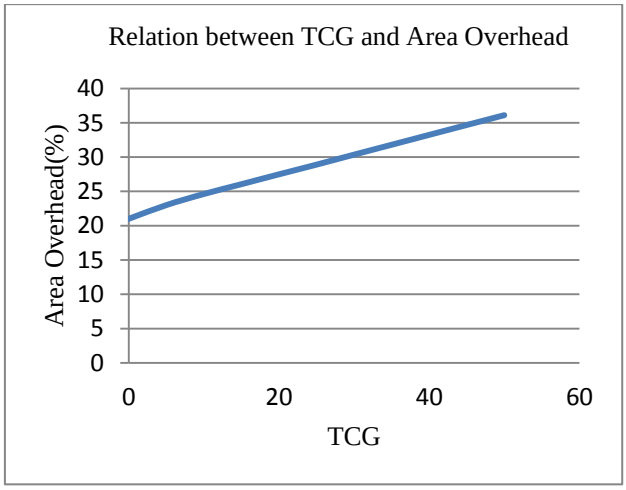

Fig.5. Relation between TCG and area overhead

5.3. Synthesis report:

Selected Device: 3s100evq100-5

Logic utilization	Used	Available	Utilization
Number of slice latches	7	9312	1%
Number of 4 input LUTs	356	9312	3%
Logic distribution			
Number of occupied slices	212	4656	4%
Number of slices containing only selected logics	212	212	100%
Number of slices containing unselected logics	0	212	0%
Total Number of 4 inputs LUTs	383	9312	4%
Number used as logics	356		
Number used as a route-thru	27		
Number of bonded IOBs	24	66	36%
Total equivalent gate count for design	3337		
Additional JTAG gate count for IOBs	1152		

Table.2 device utilization

Table.2device utilization shows that this work utilizes less number of gate counts for design i.e 3337, which indicate area is reduced.

6. CONCLUSION

This work presents BISDC architecture for self-detection and self-correction of errors of PEs in an MECA. Based on the error detection correction concepts of RQ codes, this paper also presents the corresponding definitions used in designing the BISD and BISC circuits to achieve self-detection and self-correction operations. From synthesis report we can say that the total gate count is 3337, which reveals that the area is reduced. Thus the Performance evaluation illustrates that the proposed BISDC architecture effectively achieves self-detection and self-correction capabilities with minimal area. The Functional-simulation has been successfully carried out with the results matching with expected ones. The design functional verification and Synthesis is done by using Xilinx-ISE/XST.

References

[1] Y. W. Huang, B. Y. Hsieh, S. Y. Chien, S. Y. Ma, and L. G.Chen,"Analysis and complexity reduction of multiple reference frames motion estimation in H.264/AVC," IEEE Trans. Circuits Syst. Video Technol., vol. 16, no. 4, pp. 507–522, Apr. 2006.

[2] T. H. Wu, Y. L. Tsai, and S. J. Chang, "An efficient design-for-testability scheme for motion estimation in H.264/AVC," in Proc.Int. Symp.VLSI Design, Autom. Test, Apr. 2007, pp. 1–4.

[3] M. Y. Dong, S. H. Yang, and S. K. Lu, "Design-for-testability techniques for motion estimation computing arrays," in Proc. Int.Conf.Commun., Circuits Syst., May 2008, pp. 1188–1191.

[4] Y. S. Huang, C. J. Yang, and C. L. Hsu, "C-testable motion estimation design for video coding systems," J. Electron. Sci Technol., vol. 7, no.4, pp. 370–374, Dec. 2009.

[5] J. F. Lin, J. C. Yeh, R. F. Hung, and C. W. Wu, "A built-in self-repair design for RAMs with 2-D redundancy," IEEE Trans.Vary Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp.742–745, Jun. 2005.

[6] D. P. Vasudevan, P. K. Lala, and J. P. Parkerson, "Self checking carryselect adder design based on two-rail encoding," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 12, pp.2696–2705, Dec. 2007.

[7] S. J. Piestrak, D. Bakalis, and X. Kavousianos, "On the design of selftesting checkers for modified Berger codes," in Proc. IEEE Int. WorkshopOn-Line Testing, Jul. 2001, pp. 153–157.

[8] D. K. Park, H. M. Cho, S. B. Cho, and J. H. Lee, "A fast motion estimation algorithm for SAD optimization in sub-pixel," in Proc. Int. Symp. Integr. Circuits, Sep. 2007, pp. 528–531