www.ijecs.in
International Journal Of Engineering And Computer Science ISSN:2319-7242
Volume2 Issue 8 August, 2013 Page No. 2544-2548

Comparative Analysis of CMOS Transmission Gate Based Adders

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***Abstract*: The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. In realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. There always exists a trade-off between the design parameters such as speed, power consumption, and area We designed three different types of 4-bit transmission gate based adders namely Ripple Carry Adder, Carry Select Adder and Carry Lookahead Adder We compared the different adders on basis of no. of transistors, the average power consumption and delay. The simulation results are taken for 180nm technology with the help of Tanner (T-spice) simulation tool.**

***Keywords*:** Transmission Gate, adder, CMOS, delay, power

1.Introduction

Adders are key components in digital design, performing not only addition operations, but also many other functions such as subtraction, multiplication and division. Adder is a digital circuit that performs addition of numbers. In modern computers adders are part of the arithmetic logic unit (ALU) where other operations are performed. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area. In this paper Transmission Gate Based 4-bit different adder circuit design styles are considered, describing their advantages and limitations. The use of transmission gates eliminates the undesirable threshold voltage effects which give rise to loss of logic levels in pass-transistors.

The rest of the paper is organized as follows: Adder architectures are discussed in section II. Power consumption in CMOS circuits are discussed in chapter III. Simulation Results are discussed in chapter IV. Conclusions are discussed in section V.

2.Adder Architectures

2.1. Ripple Carry Adder (RCA)

An n-bit ripple carry adder consists of 'n' full adders with the carry signal that ripples from one full-adder stage to the next, from LSB to MSB. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a C_{in} which is the C_{out} of the previous adder. Addition of k-bit numbers can be completed in k clock cycles. A 4-bit ripple carry adder structures is shown in Figure 1.

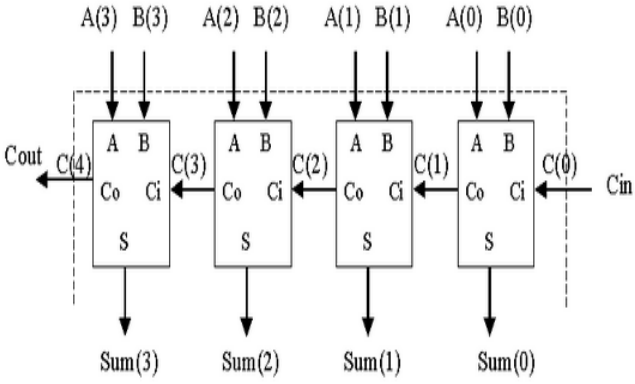

Figure 1. Structure of 4- Bit Ripple Carry Adder

The ripple-carry adder has many advantages like low power consumption, low area and simple layout. The ripple-carry adder is a good baseline design for comparison with other adders. The drawback of the ripple carry adder, though, is its slow speed because each full adder must wait for the carry bit to be calculated from the previous full adder. The delay of the adder is linearly dependent on the bit-width (N) of the adder. The critical path of the ripple carry adder consists of the carry chain from the first full adder to the last. Therefore, during circuit-level design, the carry signal is frequently assigned to the transistor closest to the gate output for the carry computation.

2.2.Carry Select Adder

In order to improve the shortcoming of carry ripple adder to remove linear dependency between computation delay time and input word length, carry select adder is presented in Figure 2.

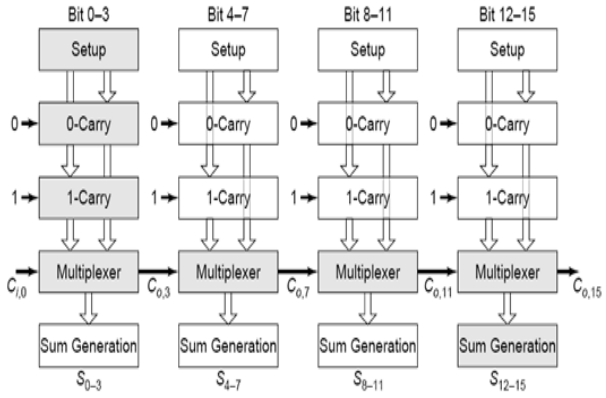

Figure 2. The 16-bit carry select adder is divided into 4 parts, while each part consists of a duplicated 4-bit carry ripple adder pair.

The carry select adder divides the carry ripple adder into M parts, while each part consists of a duplicated (N/M)-bit carry ripple adder pair . This duplicated carry ripple adder pair is to anticipate both possible carry input values, where one carry ripple adder is calculated as carry input value is logic "0" and another carry ripple adder is calculated as carry input value is logic "1". When the actual carry input is ready, either the result of carry "0" path or the result of carry "1" path is selected by the multiplexer according to its carry input value. This reduces the delay of carry propagation

2.3. Carry Lookahead Adders

One widely used approach employs the principle of carry look-ahead solves the problem of delay in carry propagation by calculating the carry signals in advance, based on the input signals. This type of adder circuit is called as carry look-ahead adder (CLA adder). To reduce the computation time, faster ways to add two binary numbers by using carry look ahead adders. It is done by creating two signals (P and G) for each bit position, based on if a carry is propagated through from a less significant bit position (at least one input is a '1'), a carry is generated in that bit position (both inputs are '1'), or if a carry is killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half-adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created.

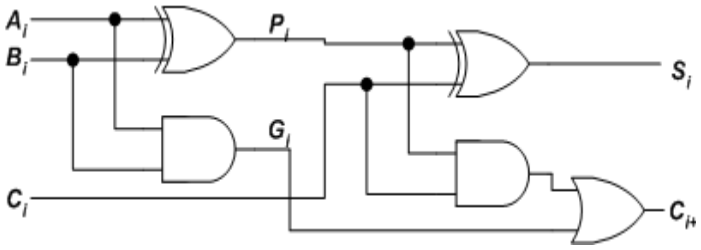

Figure 3. Adder Block Diagram Using Propagate and Generate signals

In this circuit, the 2 internal Signals Pi and Gi are given by:

$P_i=A_i \oplus B_i$

$G_i=A_iB_i$

The output sum and carry can be defined as :

$S_i = P_i \oplus C_i$

$C_{i+1}=G_i+P_iC_i$

The Boolean expression of the carry outputs of various stages can be written as follows:

C1 = G0 + P0C0

C2 = G1 + P1C1 = G1 + P1 (G0 + P0C0)

= G1 + P1G0 + P1P0C0

C3 = G2 + P2C2 = G2 + P2G1 + P2P1G0 + P2P1P0C0

C4 = G3 + P3C3

= G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C0

In general, the ith carry output is expressed in the form Ci = Fi (P's, G's , C0).

In other words, each carry signal is expressed as a direct SOP function of C0 rather than its preceding carry signal. Since the Boolean expression for each output carry is expressed in SOP form, it can be implemented in two-level circuits. The 2-level implementation of the carry signals has a propagation delay of 2 gates, i.e., 2τ. The 4-bit carry look-ahead (CLA) adder consists of 3 levels of logic. The 4 Sum signals (S0, S1, S2 & S3) will all be valid after a total delay of 4τ compared to a delay of (2n+1)τ for Ripple Carry adders. For a 4-bit adder (n = 4), the Ripple Carry adder delay is 9τ. The disadvantage of the CLA adders is that the carry expressions (and hence logic) become quite complex for more than 4 bits. Thus, CLA adders are usually implemented as 4-bit modules that are used to build larger size adders.

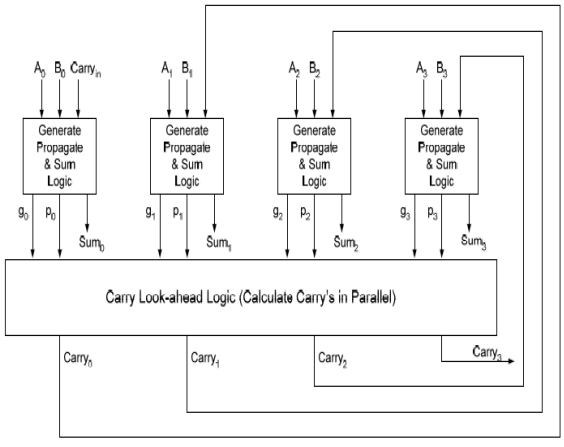

Figure 4. Structure of 4-Bit Carry Look Ahead Adder

3.Power Consumption in CMOS

There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation [1].

$$P_{total} = P_{switching} + P_{short\text{-}circuit} + P_{leakage} = (\alpha 0 \rightarrow 1 \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd}) \quad (1)$$

The first term represents the switching component of power, where C is the load capacitance, f_{clk} is the clock frequency and $\alpha 0 \rightarrow 1$ is the node transition activity factor. The second term is due to the direct path short circuit currents, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations. However, while supply voltage reduction is the most effective way to reduce the power consumption, such a reduction requires new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching, low power can also be achieved by reducing the glitches of the circuit.

4.Simulation Results

The Table 1 shows that the Ripple Carry Adder is made up of 72 transistors that is less than half the number of transistors that are required in Carry Select Adder and Carry Look Ahead Adder. The power results show that power consumption is less in Ripple Carry Adder. So we have reduced area and power consumption to a large extent in Ripple Carry Adder with reduction in speed. The delay in the Carry Look Ahead Adder is less than the Ripple Carry Adder and Carry Select Adder .The results are calculated for 0.18µm length for NMOS and PMOS at supply voltage of 1.8 volts.

Table 1.Comparison of 4-Bit Adders

Design Style	No. of Transistors	Avg. Power Consumption watts	Delay at Sum nsec	Delay at Carry nsec
Ripple Carry Adder	72	1.22×10^{-5}	0.98	3.24
Carry Select Adder	174	4.30×10^{-5}	0.87	1.30
Carry Lookahead Adder	188	8.47×10^{-5}	0.55	0.41

Figure 5 shows the variation of Avg. Power Consumed in different 4-bit adders with variation of width of the NMOS transistor for 0.18µm length for NMOS and PMOS for 180nm technology. The supply voltage used is 1.8 volts.The graph shows that power consumed by all the three types of adders increases with the increase in width of the NMOS transistor

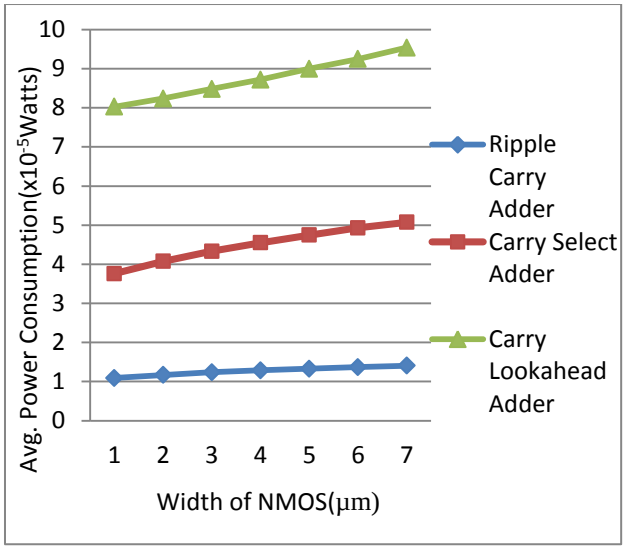

Figure 5. Variation of Avg. Power Consumed of 4-Bit Adders With Width of NMOS

Figure 6 shows the variation of Avg. Power Consumed in different 4-bit adders with variation of width of the PMOS transistor for 0.18µm length for NMOS and PMOS for 180nm technology. The supply voltage used is 1.8 volts. Graph shows that power consumed by all the three types of adders increases with the increase in width of the NMOS transistor

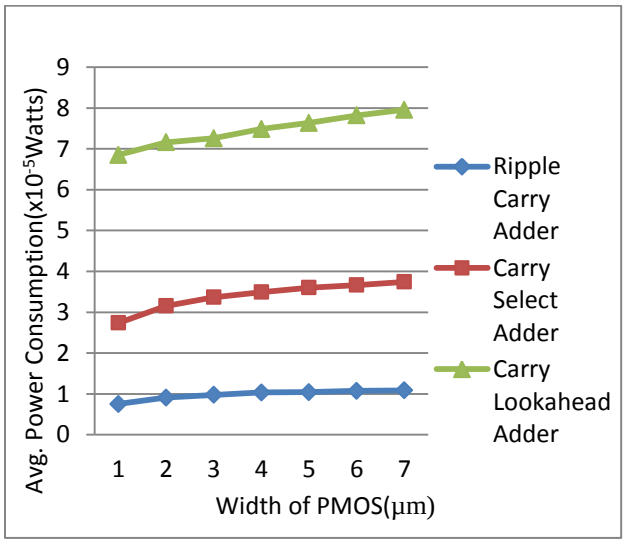

Figure 6.Variation of Avg. Power Consumed of 4-Bit Adders with Width of PMOS

5.Conclusion

In this paper a comparison among the most suitable topologies of 4-bit different adders have been carried out. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. Power consumption of a transistor can be reduced by reducing the length and width of the transistor. In this paper we conclude that power dissipation in Transmission Gate based Ripple Carry Adders is very less as compared to Transmission Gate based Carry Select Adder and Transmission Gate based Carry Look

Ahead Adder. So where power is an important criterion there we should prefer Ripple Carry Adder. Delay in Carry Look Ahead Adder is less than Ripple Carry Adder and Carry Select Adder. So where high speed adders are required, we should use Carry Lookahead Adders.

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