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Design And Analysis Of High Speed, Low Power And Area Efficientdct Architecture For Multimedia Applicationsimplemented Oncadence 180nm

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Abstract: In this paper proposed power and area efficient discrete cosine transform (DCT) architecture for multimedia applications. This paper Implemented conventional DCT and multiplier less DCT's by less number of adders/subtracter and multipliers. Area and power achieved by reducing mathematical operations. Number of cells, cell area, internal power, net power, leakage power, switching power reduced compared to conventional DCT. Power delay product of both conventional DCT and multiplier less DCT's are 19.8mJ, 19.7mJ and 10.8 mJ respectively. The proposed DCT and conventional DCT are implemented on cadence RTL compiler 180nm.

Keywords: c*onventional DCT, multiplier less DCT, PDP*

I. INTRODUCTION

Due to requirement of low power and low hardware cost, the implementation of efficient discrete cosine transformation is challenging problem, the important function in data compression. Data compression is most important for efficient transmission and storage of data. Therefore development of optimized technique for data compression has become quite necessary.The discrete cosine transform is most important architecture for image compression. Most of the multimedia applications required high speed data compression algorithms, such as jpeg, MPEG and H.26X[1-2]. Our contributions are as follows.

- Implementing conventional DCT(discrete cosine transform) and multiplier less DCT's algorithms.
- Comparison of DCT(discrete cosine transform) algorithms in terms of power, area, number of cell, power delay product, leakage power, switching power, net power.
- Finding high speed DCT(discrete cosine transform) algorithm for multimedia applications.

To achieve efficient algorithms, many researchers have been implemented multiplier based DCT's. The need of DCT is plays key in signal processing, especially portable devices like mobile, laptops. DCT(discrete cosine transform) has been adopted many DSP algorithms such as DFT(Discrete Fourier Transform), convolution.

DCT (discrete cosine transforms) is slow to compute since it takes sizable amount of multiplications. Many DCT (discrete cosine transform) algorithms have been implemented [3] to reduce the number of multiplication. It is also been proposed that the less multiplications for the computation of DCT (discrete cosine transform) [4]. In this paper have been presented conventional DCT(discrete cosine transforms) and multiplier less DCT's, comparing the results of Architectures.

This paper is arranged as following, section I is containing introduction of DCT. Section II involves conventional DCT(discrete cosine transform) and Multiplier less DCT(discrete cosine transform) algorithms. Section III discussed results. Section IV involves conclusion and discussion. Last section involves references.

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II. IMPLEMENTATION OF CONVENTIONAL DCT AND MULTIPLIER LESS DCT

Many Multiplier less DCT's are proposed [5-6], they were have been used direct factorization method. The general N point DCT is shown below.

$$X(k)=\sum_{n=0}^{n=N-1} e(r)Y(n)\cos(\frac{(2n+1)k\Pi}{N}), k=o,1,2,....N-1 \qquad (1)$$

Where

$$e(r)=\begin{cases}\frac{1}{\sqrt{2}}, & \text{if } k=0\\ 1, & \text{otherwise}\end{cases}$$

Where Y (n) is input sequence, if we implement direct method it need N(N-1) multipliers, so we are using trigonometric functions to reduce the multiplications instead of direct multiplications. The matrix multiplication of the 8 point DCT is shown below.

$$\begin{bmatrix}X(0)\\X(1)\\X(2)\\X(3)\\X(4)\\X(5)\\X(6)\\X(7)\end{bmatrix}=\begin{bmatrix}c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4\\ c_1 & c_3 & c_5 & c_7 & c_9 & c_{11} & c_{13} & c_{15}\\ c_2 & c_6 & c_{10} & c_{14} & c_{18} & c_{22} & c_{26} & c_{30}\\ c_3 & c_9 & c_{15} & c_{21} & c_{27} & c_1 & c_7 & c_{13}\\ c_4 & c_{12} & c_{20} & c_{28} & c_4 & c_{12} & c_{20} & c_{28}\\ c_5 & c_{15} & c_{25} & c_3 & c_{13} & c_{23} & c_1 & c_{11}\\ c_6 & c_{18} & c_{30} & c_{10} & c_{22} & c_2 & c_{14} & c_{26}\\ c_7 & c_{21} & c_3 & c_{17} & c_{31} & c_{13} & c_{27} & c_9\end{bmatrix}\begin{bmatrix}Y(0)\\Y(1)\\Y(2)\\Y(3)\\Y(4)\\Y(5)\\Y(6)\\Y(7)\end{bmatrix} \qquad (2)$$

Where $c_i = \cos\frac{i\pi}{16}$, i=0, 1, 2, 3…… N-1

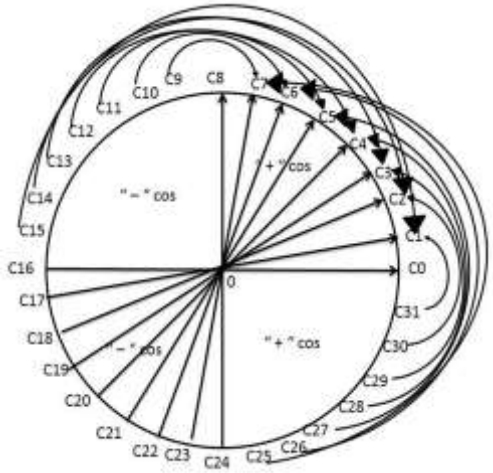

Fig.1.Quadrant circle for reducing twiddle factor.

From the quadrants circle the $C_i$can be reduced as f

$$\begin{bmatrix}X(0)\\X(1)\\X(2)\\X(3)\\X(4)\\X(5)\\X(6)\\X(7)\end{bmatrix}=\begin{bmatrix}c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4\\ c_1 & c_3 & c_5 & c_7 & -c_7 & -c_5 & -c_3 & -c_1\\ c_2 & c_6 & -c_6 & -c_2 & -c_2 & -c_6 & c_6 & c_2\\ c_3 & -c_7 & -c_1 & -c_5 & c_5 & c_1 & c_7 & -c_3\\ c_4 & -c_4 & -c_4 & c_4 & c_4 & -c_4 & -c_4 & c_4\\ c_5 & -c_1 & c_7 & c_3 & -c_3 & -c_7 & c_1 & -c_5\\ c_6 & -c_2 & c_2 & -c_6 & c_6 & c_2 & -c_2 & c_6\\ c_7 & -c_5 & c_3 & -c_1 & c_1 & -c_3 & c_5 & -c_7\end{bmatrix}\begin{bmatrix}Y(0)\\Y(1)\\Y(2)\\Y(3)\\Y(4)\\Y(5)\\Y(6)\\Y(7)\end{bmatrix} \qquad (3)$$

From the above matrix we can re write the equations

X(0)=C_4[Y(0)+Y(1)+Y(2)+Y(3)+Y(4)+Y(5)+Y(6)+Y(7)]

X(1)=C_1[Y(0)–Y(7)]+C_3[Y(1)–Y(6)]+C_5[Y(2)Y(5)]+C_7[Y(3) – Y(4)]

X(2)=C_2[Y(0)–Y(3)–Y(4)+Y(7)]+C_6[Y(1)–Y(2)Y(5)+Y(6)]

X(3)=C_3[Y(0)–Y(7)]+C_7[Y(1)–Y(6)]+C_1[Y(2)Y(5)]+C_5[Y(3) –Y(4)]

X(4)=C_4[Y(0)-Y(1)-Y(2)+Y(3)+Y(4)-Y(5)-Y(6)+Y(7)]

X(5)=C_5[Y(0)–Y(7)]+C_1[Y(1)–Y(6)]+C_7[Y(2)-Y(5)]+C_3[Y(3) –Y(4)]

X(6)=C_6[Y(0)–Y(3)–Y(4)+Y(7)]+C_2[Y(1)–Y(2)Y(5)+Y(6)]

X(7)=C_7[Y(0)–Y(7)]+C_5[Y(1)–Y(6)]+C_3[Y(2)–Y(5)]+C_1[Y(3) –Y(4)]

Where

$C_4=\frac{1}{2}\cos\frac{\pi}{4}$, $C_2=\frac{1}{2}\cos\frac{\pi}{8}$, $C_6=\frac{1}{2}\cos\frac{3\pi}{8}$

$C_1=\frac{1}{2}\cos\frac{\pi}{16}$, $C_3=\frac{1}{2}\cos\frac{3\pi}{16}$, $C_5=\frac{1}{2}\cos\frac{5\pi}{16}$,

$C_7=\frac{1}{2}\cos\frac{7\pi}{16}$

Implementation of above equations needs 21 multipliers and 28 add/sub. The fig 2 shows butterfly structure of 21 multipliers. Using trigonometric functions the DCT algorithm can be Conventional DCT multipliers reduced to 10.

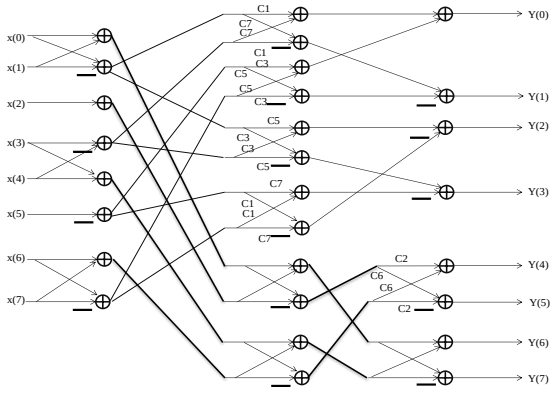

Fig. 2.conventional DCT butterfly structure [7].

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Using quadrant circle reducing the number of multiplications by 10 compared to the conventional DCT. Fig 3 shows the butterfly structure of 10 multiplier DCT.

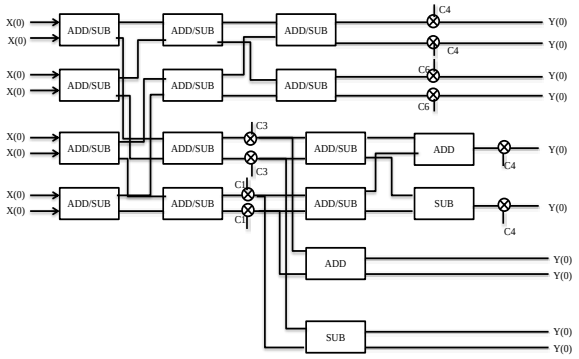

Fig.3. 10 multiplier DCT Butterfly

According to the basics of these basic characteristics, to reduce the multipliers in DCT adopting new type of transform called variant integer DCT transform [8], its transform matrix is C. in order to meet orthogonality, consider CC^Tas following

	Conventional DCT	10 Multiplier DCT	5 Multiplier DCT
Cells	52055	29507	18389
Cell Area	299717.65	173276	102821
Leakage Power (nw)	101840.93	61707	32423.49
Internal Power (nw)	4100353.85	3081873	1848927.89
Net Power (nw)	5363390.32	3987545	2548224.98
Switching power(nw)	9463744.17	7069419	4397152.88

$$J=CC^T$$

$$J=\begin{bmatrix} J_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & J_2 & 0 & J_0 & 0 & 0 & 0 & 0 \\ 0 & 0 & J_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & J_0 & 0 & J_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & J_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & J_2 & 0 & -J_0 \\ 0 & 0 & 0 & 0 & 0 & 0 & J_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & -J_0 & 0 & J_4 \end{bmatrix} \quad (4)$$

Where

$$J_O = 4(C_1C_5 - C_2C_6), J_1 = 8C_0{}^2, J_2 = 4(C_1{}^2 + C_2{}^2)$$
$$J_3 = 4(C_3{}^2 + C_4{}^2) \text{ and } J_4 = 4(C_4{}^2 + C_5{}^2)$$

CC^T is to be a diagonal matrix, to meet orthogonality J_0=0 or $C_1C_5 = C_2C_6$. From the orthogonality theorem we reduced multipliers and the fig 4 shows butterfly diagram. Using the orthogonality theorem we are reduced number of multipliers compared to the conventional DCT.

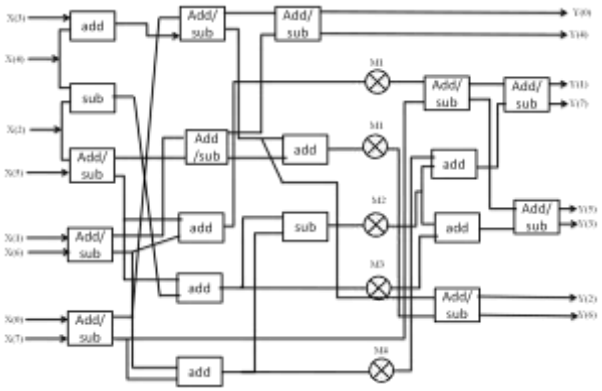

Fig.4. 5 multiplier DCT butterfly architecturefromAgostini et.al.[9].

III. RESULTS AND DISCUSSIONS

We have discussed in the above section implementation of conventional, 10 multiplier DCT and 5 multiplier DCT. The results of these algorithms discussed as shown in the Table 1, in terms of cell area, cells, leakage power, internal power, net power, switching power.

TABLE 1Comparison of Conventional DCT, 10 Multiplier DCT and 5 Multiplier DCT

Table 2 shows the delay and power delay product(PDP) of conventional, 10 Multiplier DCT and 5 Multiplier DCT, 5 Multiplier DCT having less power delay product.

TABLE 2Delay and PDP of DCT algorithms

	Conventional DCT	10Multiplier DCT	5Multiplier DCT
Delay (ps)	3775.9	4950	4267.8
Power Delay Product (PDP)(mJ)	19.8	19.7	10.7

The graphs are showing differentiate Conventional DCT, 10 Multiplier DCT and 5 Multiplier DCT in terms of area, power and PDP.

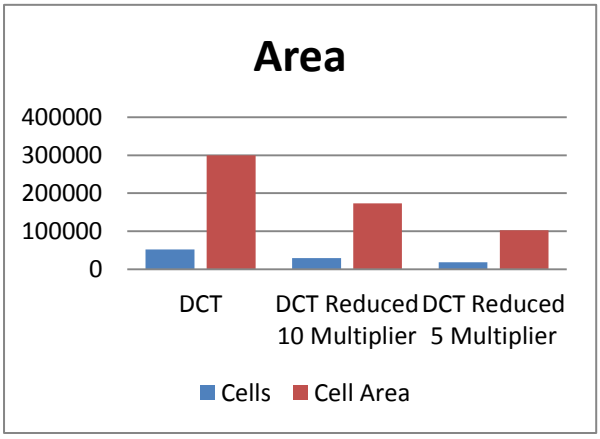

Fig.5.Areaof conventional, 10 multiplier and 5 multiplier DCT algorithms.

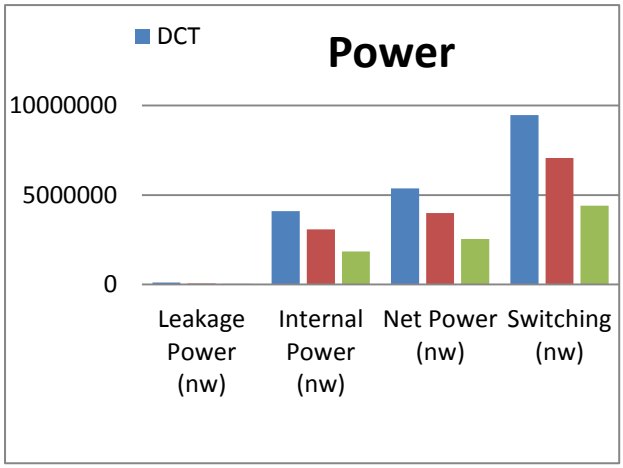

Fig. 6. Powerof conventional, 10 multiplier and 5 multiplier DCT algorithms.

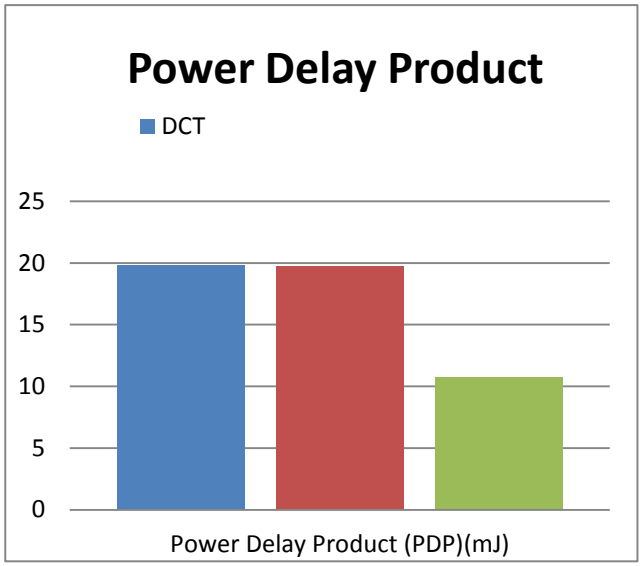

Fig. 7.Power delay product (PDP) of conventional, 10 multiplier and 5 multiplier DCT algorithms.

CONCLUSION

All the algorithms are implemented on Cadence RTL compiler 180nm.Comparing the results of Conventional DCT and proposed DCT, numbers of cells are reduced to 35%, cell area can be reduced by 34.3%, and leakage power can be reduced by31.8%. Internal power, net power and switching power reduced by 45.9%, 47.5% and 46.4% respectively. From the above results, the delay is slightly increasing but finding the power delay product (PDP) we can tell the proposed DCT is faster than the conventional DCT, it consumes less power and the area of the proposed DCT also less

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