www.ijecs.in
International Journal Of Engineering And Computer Science ISSN:2319-7242
Volume 3 Issue 12 December 2014, Page No. 9598-9601

Design of Low Power 9T Full Adder Based 4*4 Wallace Tree Multiplier

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Abstract: ***Multiplier is an important key element used for arithmetic operations in digital signal processor. Power consumption in multiplier is more when compared with adders and subtractors. So reducing the power consumption of multiplier makes a digital signal processor more efficient. A Wallace tree multiplier is an efficient high speed multiplier that multiplies two integers. Here a 4*4 Wallace tree multiplier is proposed with ten full adders. Each full adder used in this design has only nine transistor which is less in number when compared with the conventional full adders. Due to this the power consumption of full adder block is reduced, such that power consumption of 4*4 Wallace Tree Multiplier will be reduced. The proposed design is simulated using 0.12µm technology in Microwind 2 Tool and has achieved upto 50% power saving in comparison to the Wallace Tree Multiplier that has been designed using Conventional Full adder.***

Keywords: Full adder, Multiplier, Wallace Tree Multiplier, Power consumption.

1. Introduction

Due to immense increase in portable devices, power consumption is given a prior importance compared to other factors. Power consumption of a VLSI system[1] increases when the chip density is increased. Reducing the power consumption is considered to be a major design factor which reduces the heat generated in devices by cooling, increases battery life for many portable devices and also increases the operating time of a system. Reducing the power supply(Vdd) obviously reduces the energy consumption of a CMOS circuit[2]. But reducing the power supply voltage increases the delay of a circuit and decreases the driving capacity of each transistor. So without reducing the power supply voltage, power consumption can be minimized by choosing proper aspect ratio and by minimizing the transistor count required for a circuit. Adders and multipliers are the most commonly used element in microprocessor and digital signal processor for various arithmetic operations. The adder designed in this paper consists of only nine transistors[3] which has a reduced transistor count that obviously decreases the power consumption. As adder forms to be the basic building block of a multiplier, minimizing the power consumption of an adder minimizes the power consumption of a multiplier. Among the different types of multiplier, Wallace Tree multiplier[4] is chosen for the design. Wallace Tree multiplier is an efficient high speed multiplier that multiplies two integers.

2. Existing Work

Wallace Tree multiplier is an efficient hardware implementation of a digital circuit that multiplies two integers. It is a combination of half adders and full adders. The structure of Wallace Tree multiplier is explained in Figure 1. Here a 4*4 Wallace Tree multiplier is designed with ten full adders by replacing the half adder with full adders[5].

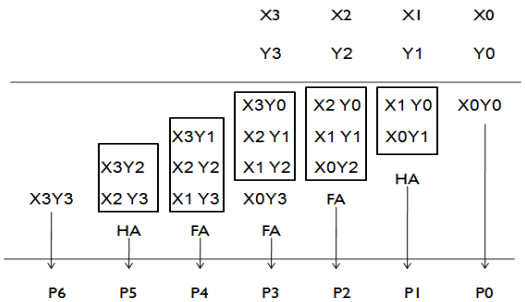

Figure 1: Structure of Wallace Tree Multiplier

Initially a 4*4 Wallace Tree multiplier is designed using a Conventional Full Adder[6]. The Conventional Complementary Metal Oxide Semiconductor full adder consists of both pull up and pull down networks. It consists of 28 transistors. The schematic diagram of 28 transistor full adder is shown in Figure 2 and a 4*4 Wallace Tree Multiplier with this 28 transistor adder design is shown in Figure 3. The design is simulated using 0.12µm technology in Microwind 2 Tool and

resulted with high power consumption due to increased transistor count.

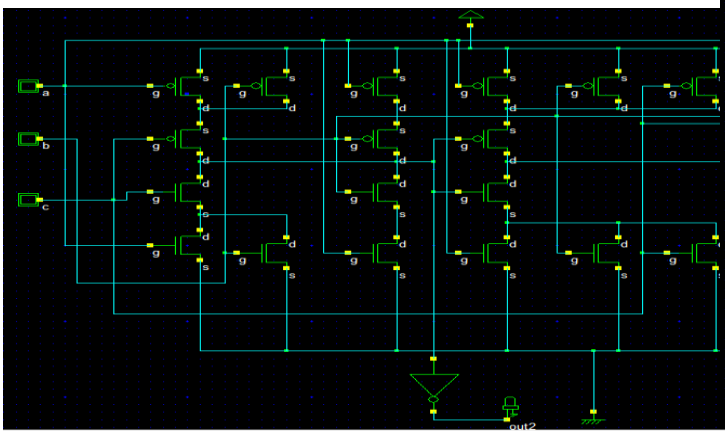

Figure 2: Schematic diagram of 28T Full Adder

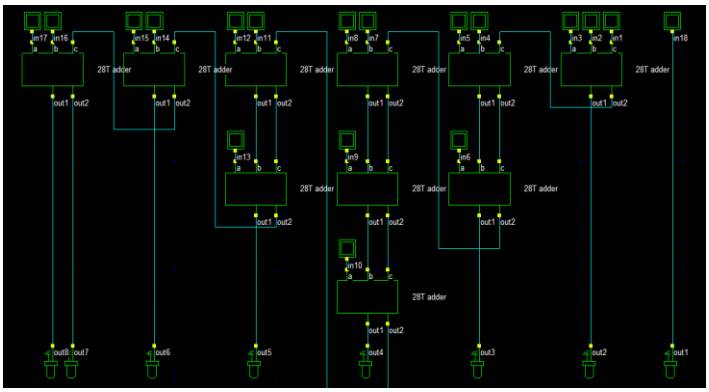

Figure 3: Schematic diagram 28T Full Adder based 4*4Wallace Tree Multiplier

Later, a 14T full adder[7] is proposed. This design is a combination of XOR-XNOR circuit and transmission gates. It do not provide enough driving power due to non full swing sum output and full swing carry output. Though it occupies less area, it consumes more power due to threshold voltage losses. But the power dissipation of 14T adder is much less than that of the conventional adder. The schematic diagram of 14T full adder is shown in Figure 4 and 4*4 Wallace Tree Multiplier with 14T full adder is shown in Figure 5. The design is simulated using 0.12µm technology in Microwind 2 Tool.

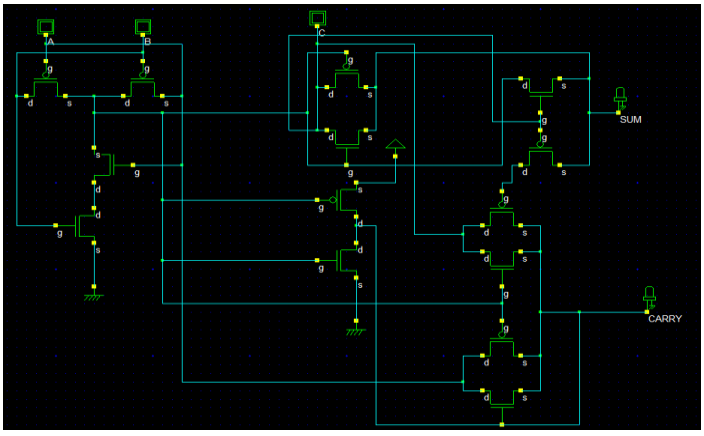

Figure 4: Schematic diagram of 14T Full Adder

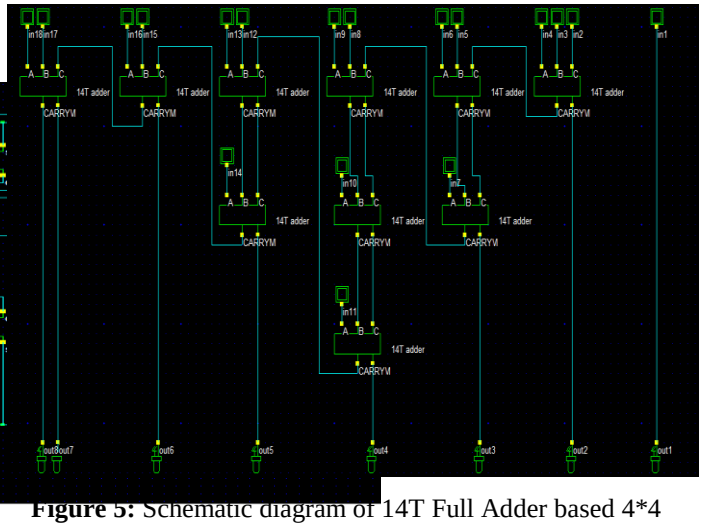

Figure 5: Schematic diagram of 14T Full Adder based 4*4 Wallace Tree Multiplier

3. Proposed Work

This proposed work presents the design of low power 4X4 Wallace Tree multiplier based on 9T full adders[8]. Based on the comparison of the existing adders[9], the 9T full adder is chosen for the design due to its low power consumption. The 9T full adder consists only one 3T XOR gate. This full adder has overcome the voltage degradation occurring due to threshold drop. This problem has overcome by increasing the aspect ratio(W/L) by making the length as constant and increasing the width. Here the 9T Full Adder is designed using 0.12µm technology in Microwind 2 Tool. The schematic diagram of 9T full adder is shown in Figure 6. Finally it is proved that reducing the transistor count decreases the power consumption of a circuit.

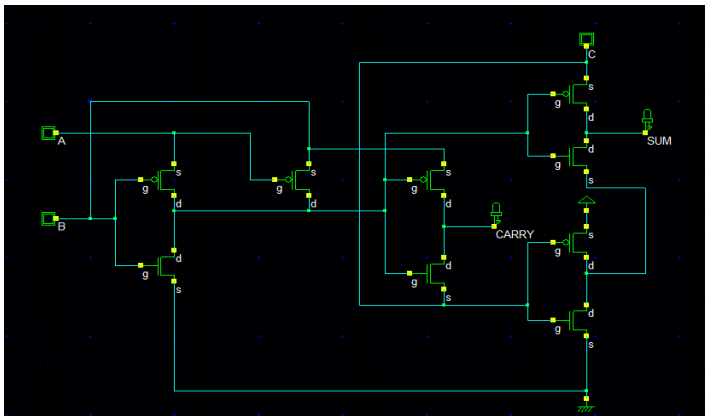

Figure6: Schematic diagram of 9T Full Adder

Though different multipliers[10] exist, here a Wallace Tree Multiplier is chosen for design due to its high performance and speed. Now a 4*4 Wallace Tree Multiplier is designed with the above simulated 9T full adder using 0.12µm technology in Microwind 2 Tool. The Wallace Tree Multiplier designed here consists of 10 nine transistor full adder. Here it is shown that reducing the transistor count, reduces the power consumption of a CMOS circuit. The schematic diagram of 4*4 Wallace Tree Multiplier based on 9T full adder is shown in Figure 7.

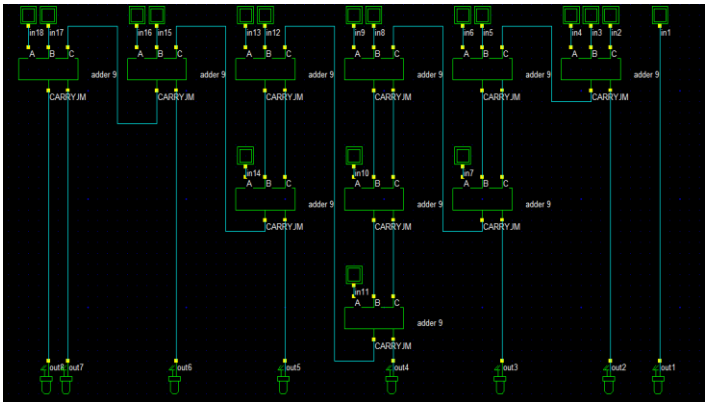

Figure 7: Schematic diagram of 9T Full Adder based 4*4 Wallace Tree Multiplier

4. Results

A Wallace Tree Multiplier based on 9T full adder has been proposed. From the result, the proposed design consumes less power when compared to the conventional full adder based Wallace Tree Multiplier. It saves upto 50% of power compared to Wallace Tree Multiplier based on conventional full adder. Using the Wallace Tree Multiplier based on 9T full adder in a Digital Signal Processor makes the system more efficient. These designs were simulated using 0.12µm technology in Microwind 2 Tool and the output waveforms and the generated layout for the proposed design are given below

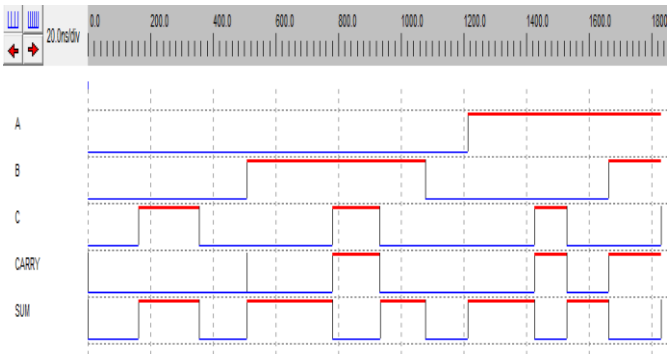

Figure 8: Simulated Waveforms of 9T Full Adder

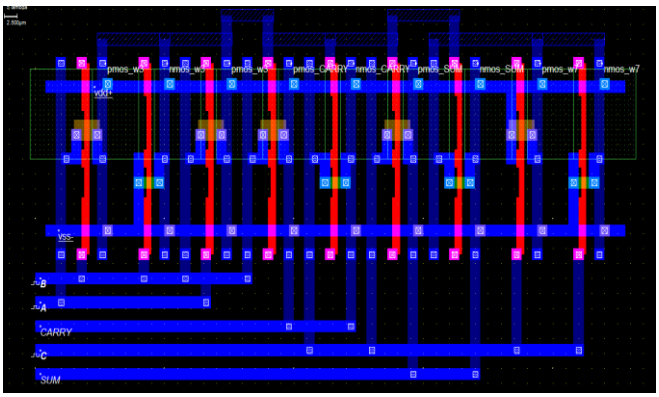

Figure 9: Layout of 9T Full Adder

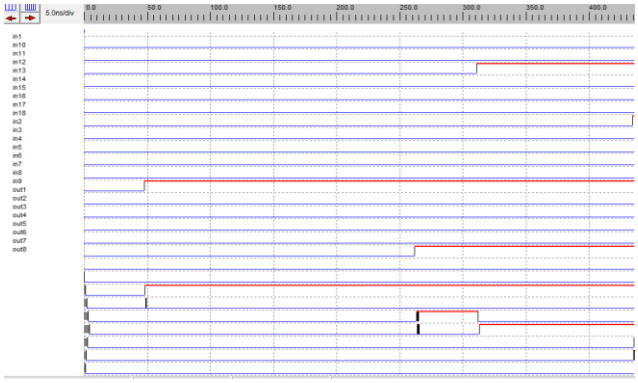

Figure 10: Simulated Waveform 9T Full Adder based4*4 Wallace Tree Multiplier

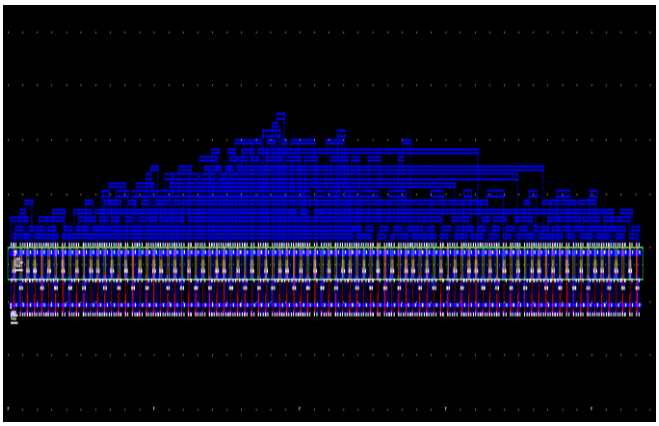

Figure 11: Layout 9T Full Adder based4*4 Wallace Tree Multiplier

5. Comparison

Table1 shows the comparative analysis between the conventional full adder, 14T full adder and 9T full adder. This analysis shows that 9T full adder has less transistor count and power consumption. Table 2 shows the comparative analysis between the Wallace tree multiplier based on conventional full adder, 14T full adder and 9T full adder. From the analysis it shows Wallace tree multiplier with 9T full adder is best suited for the low power applications as it is effective in all cases such as transistor count and power consumption.

Table 1: Comparison Table for Full Adders

	28T Full Adder	14T Full Adder	9T Full Adder
Transistor count	28	14	9
Power Consumption	0.069µw	0.112mw	7nw

Table 2: Comparison Table for Wallace Tree Multipliers

	Wallace Multiplier based on 28T Full Adder	Wallace Multiplier based on 14T Full Adder	Wallace Multiplier based on 9T Full Adder
Transistor Count	280	140	90
Power Consumption	0.544µw	0.360µw	0.295µw

6. Conclusion

In this paper, a 4*4 Wallace Tree Multiplier based on 9T full adder was designed using 0.12µm technology in Microwind 2 Tool. From the results and comparison, it has been proved that the Wallace Tree Multiplier based on 9T full adder has less power consumption. It consumes only 50% of the power when compared to other conventional full adder based Wallace Tree Multipliers. The Wallace Tree Multiplier based on 9T full adder is worth enough to make a Digital Signal Processor performance efficient.

References

[1] John P.Uymera, "Introduction to VLSI Circuits and Systems"

[2] Neil.H.E.Weste and K.Eshraghian, "Principles of CMOS VLSI Design," Addison-Wesley,1993.

[3] SubodhWariya, Rajendra Kumar Nagaria and Sudarshan Tiwari, "Performance Analysis of High Speed Hybrid CMOS Full Adder Circuits for Low Voltage VLSI Design," Hindawi Publishing Corporation, VLSI Design, Volume 2012.

[4] V.Alekhya andB.Srinivas, "Architectural Level Power Optimization Techniques for Multipliers," International Journal of Engineering Trends and Technology, Volume3, Issue5, 2012.

[5] R.Naveen,K.Thanushkodi and C.Saranya,"Leakage power reduction in Wallace tree multiplier using current comparison domino logic",JATIT,Volume 55,No 1,2013.

[6] Y.SunilGavaskar Reddy and V.V.G.S. Rajendra Prasad, "Power Comparison of CMOS and Adiabatic Full Adder Circuits," International Journal of VLSI Design and Communication Systems, Vol.2, No.3,September 2011

[7] M. Clerc, SubodhWariya, Rajendra Kumar Nagaria and Sudarshan Tiwari, "Comparative Performance Analysis of XOR-XNOR Function based High-Speed CMOS Full International Journal of VLSI Design and Communication Systems, Vol.3, No.2, April 2012.

[8] Shiwani Singh, Tripti Sharma, K.G.Sharma and Prof.B.P.Singh, "Low Power 1-Bit 9T Full Adder Cell using XNOR Logic," Proc. of the Intl. Conf. On Advances in Computer Science and Electronics Engineering.

[9] Pradeep Kumar, "Existing Full Adders and their Comparison on the basis of Simulation Result and to Design a Improved LPFA," International Journal of Engineering Research and Applications, Vol.2, Issue 6, November-December 2012.

[10] SaroRamya S, Sakthivel S, Prakash S P, "Design and Comparison of Array and Tree Multiplier Using Different Logic Styles," International Journal of Engineering and Innovative Technology, Volume 2, Issue 7, January 2013.