www.ijecs.in
International Journal Of Engineering And Computer Science ISSN:2319-7242
Volume- 3 Issue -3 March, 2014 Page No. 5004-5007

Low-Voltage, High Frequency CMOS Analog Multiplier

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Abstract— **A new CMOS voltage-mode Four-quadrant analog Multiplier is proposed and analyzed by applying inputs signals to set of Summation circuit and substractor. Based on the proposed multiplier circuit, a low voltage high performance CMOS four quadrant analog multiplier is designed and simulated by using 0.35 micron technology. The measured 3dB bandwidth is 15 MHz. Simple structure, low-voltage, low power, and high performance makes the proposed multiplier quite feasible in many applications**

Keywords— **low voltage, low power, high frequency.**

I. INTRODUCTION

Analog multipliers are important circuit blocks for many applications such as frequency mixers, variable frequency oscillators, adaptive filters, neural networks automatic gain control, amplitude modulation, etc. In order to improve the overall power efficiency of such application which is now regularly required for modern analog and mixed signal design dedicated for portable equipments, the analog multiplier to be used must be able to operate under a reduced supply voltage and consume low current.

Four quadrant analog multipliers are widely used in contemporary VLSI chips for non-linear operations, modulation/demodulation as well as frequency conversion.

The basic functionality of the multiplier is to deliver output signal ***v0*** proportional to the product of two input voltages V_1 and V_2:

$$V0=km\,.\,V_1.\,V_2$$

Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar CMOS technologies [6],[7].

Multipliers are classified based on its MOS region of operation. One type is analog multiplier circuit based on square-law characteristics of MOS transistor [2, 3, 6]. The square-law characteristics of MOS multiplier can be realized easily since the squaring function can be obtained from the inherent square law of the MOS transistor operating in the saturation or triode region [3]-[5].

The multiplier proposed in this paper use analog adder circuit with squaring circuits to get the quarter square algebraic identity.

II. CIRCUIT DESCRIPTION

The multiplier proposed in this paper has great advantage as it cancels all non linear components at the output of the multiplier .the multiplier configuration is achieved using quarter square identity, to implement the quarter square algebraic identity we use a summer and squarer circuit.

$$(V_1+V_2)^2 - (V_1-V_2)^2 = 4V_1V_2. \quad (1)$$

Where V_1 & V_2 are the input voltages. From the above relation the circuit needs summer, subtracter and squarer circuit to implement the multiplier.

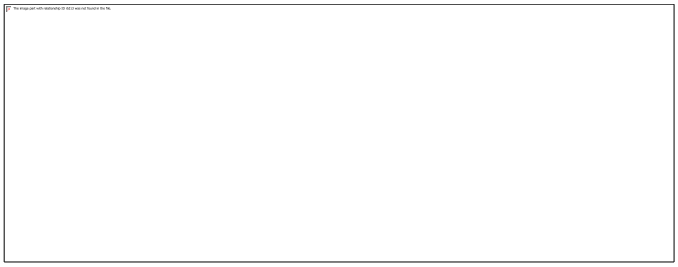

Fig.1 Proposed Multiplier

A. **SUMMING CIRCUIT:**

In the following circuit analysis, it is assumed that the drain current of the MOS device in saturation is given by the following equation (2) &(3)

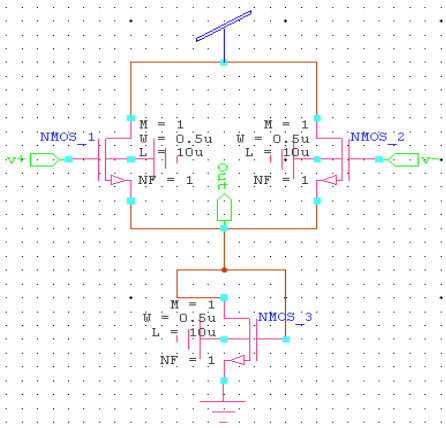

Fig. 2: Squaring Circuit

Now by applying the input voltages V_1, the current flowing through the drain terminal of the MOS transistor is given as,

$$I_{D1}=0.5 \quad u_{n1}C_{OX1} \quad W/L_1(V_{GS1}-V_{Tn1})^2 \quad (2)$$

$$I_{D2}=0.5 \quad u_{n2}C_{OX2} \quad W/L_2(V_{GS2}-V_{Tn2})^2 \quad (3)$$

Where I_{D1} is the drain current flowing through NMOS _1& I_{D2} is the current flowing through NMOS_2, & V_{Tn} is threshold voltage of the transistor.

From the circuit we can conclude that,

$$I_{SUM}=I_{D1}+I_{D2} \quad (4)$$

$$=K/2[(V-V_{OUT}-V_{Tn})^2 + (-V-V_{OUT}-V_{Tn})^2]$$

$$=K[V^4+2 \quad V^2(V_{SS}+ \quad 2V_{Tn})^2+ \quad (V_{SS}+2V_{Tn})^4]/ \quad 4(V_{SS} +2V_{Tn})^2$$

The voltage at V_{out} can be derived from using small signal model that is:

$$V_{OUT}= K/2gm\ V^2 + K/4g_m(V_{SS}+2V_{Tn})^2 \quad (5)$$

B. **SUBTRACTION CIRCUIT & SUMMATION CIRCUIT:**

For getting the difference & sum of two input signal V1 & V2, they are applied to the subtraction circuit & summation circuit respectively. The relationship of the drain current of transistors M1-M2, M3-M4 is:

B.1) ***Subtracter Circuit:***

$$I_{D1}= I_{D2}$$

$$I_{D3} = I_{D4}$$

$$K\ (V_1- V_{OUT+} -V_{Tn})^2 = K\ (V_2- V_{SS} -V_{Tn})^2$$

$$K\ (-V_1- V_{OUT-} -V_{Tn})^2 = K\ (-V_2- V_{SS} -V_{Tn})^2$$

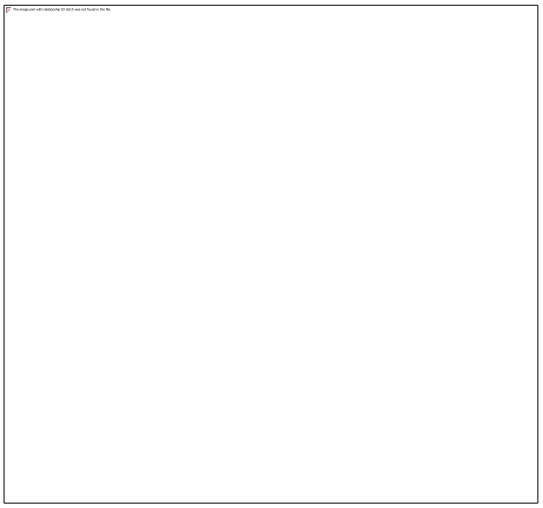

Fig3 A: Subtraction Circuit

The output voltage of signal subtraction circuit is:

$$V_{OUT+} =V_1 –V_2 +V_{SS}$$

$$V_{OUT-} =-V_1+V_2 +V_{SS}$$

$$V_{OUT} = V_{OUT+} -V_{OUT-} = 2(V_1 –V_2) \quad (6)$$

B.2*) Summation Circuit:*

The relationship of the drain current of transistors M1-M2, M3-M4 is:

$$I_{D5} = I_{D6}$$

$$I_{D7} = I_{D8}$$

$$K (V_1 - V_{OUT+} - V_{Tn})^2 = K (-V_2 - V_{SS} - V_{Tn})^2$$

$$K (-V_1 - V_{OUT-} - V_{Tn})^2 = K (V_2 - V_{SS} - V_{Tn})^2$$

The output voltage of signal subtraction circuit is:

$$V_{OUT+} = V_1 + V_2 + V_{SS}$$

$$V_{OUT-} = -V_1 - V_2 + V_{SS}$$

$$V_{OUT} = V_{OUT+} - V_{OUT-} = 2(V_1 + V_2) \quad (7)$$

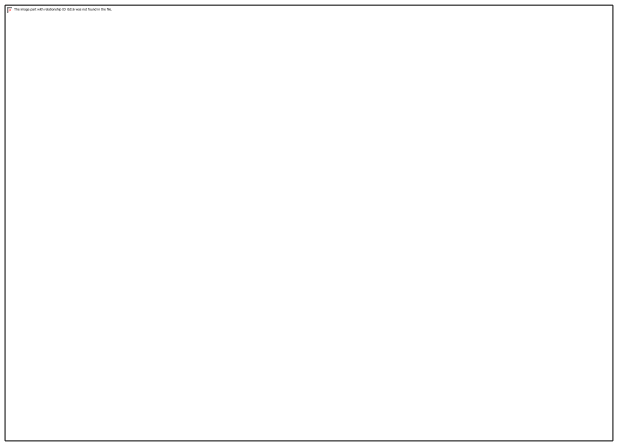

Fig.3 B: Summation Circuit

C. **MULTIPLIER**

Employing the squaring circuit of fig.2 and the summation – subtraction circuit of Fig.3A & Fig. 3B. The subtraction between squarer summing and squarer difference gives the result of multiplier in voltage mode.

$$V_{OUT} = K/2g_m (V_{OUT(SUM)}^2 - V_{OUT(SUB)}^2)$$

$$V_{OUT} = K/2g_m [(2(V_1+V_2))^2 - (2(V_1 - V_2))^2]$$

$$V_{OUT} = \beta V_1 V_2$$

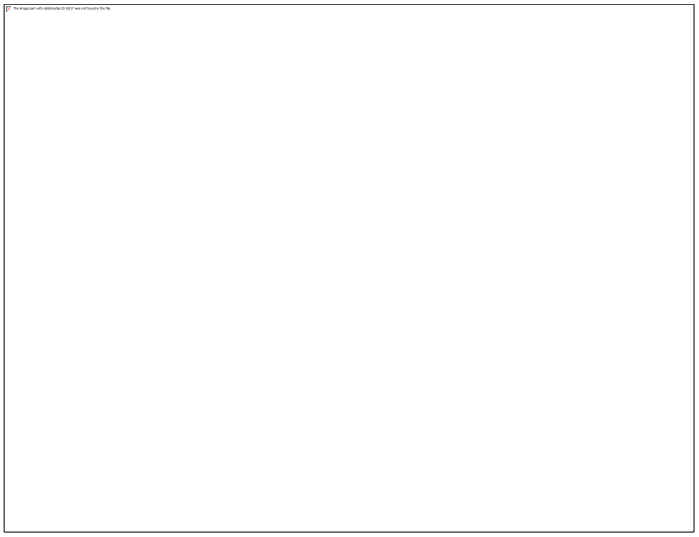

Fig.4: Proposed Multiplier Circuit

III. SIMULATION RESULT

The proposed four quadrant multiplier shown in fig .4 has been simulated with TSPICE using 0.35micron level 3 process. The power supply voltage is ±1V.

Fig.5 shows the waveform for amplitude modulation as one of the application of a multiplier. The modulation is performed when the input voltage v1 & v2 are 100 KHz & 1 MHz with the peak amplitude of 400mV.

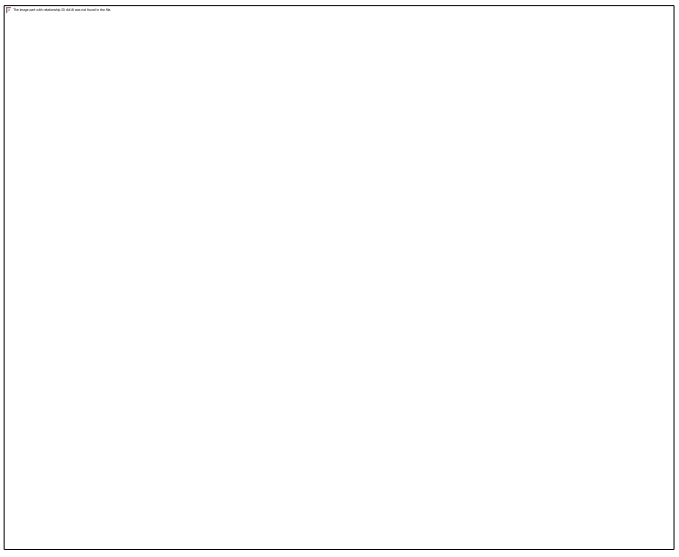

Fig 5: Transient response of the four quadrant multiplier

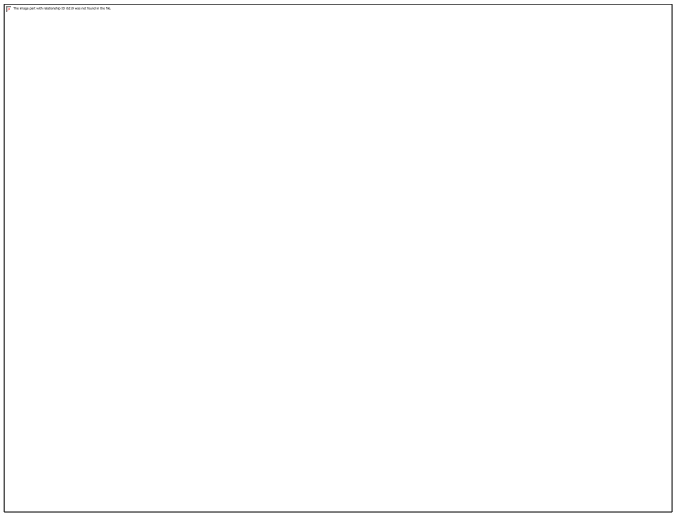

Fig.6: Frequency response of the four quadrant multiplier.

The error voltage is measured within the range ±400mV for V_1, while the other input V_2 varies from ±400mV. The power consumption avg_power =1.8819e-005. The proposed circuit achieves the output without using the passive component i.e. resistors.

IV. CONCLUSION

A voltage-mode four-quadrant analog multiplier based on simple summation-subtraction and squaring circuits is proposed. The circuit is based on the simple square mathematics model that implements simple operational trans conductance amplifier pairs and squaring circuit. It achieves the multiplied output signal in voltage form without using resistors. The design uses 0.35micron CMOS process and the performance has been demonstrated by using TSPICE.

REFERENCES

[1] Montree Kumngern (2013), "A DXCCII-Based Four-Quadrant Multiplier", 2013 IEEE 7th International Power Engineering and Optimization Conference (PEOCO2013), Langkawi, Malaysia. 3-4 June, 2013.

[2] Nipa B. Modi, Priyesh P. Gandhi (2013), "Four Quadrant Analog Multiplier with VCVS in Deep-submicron Technology", Proceedings of2013 IEEE Conference on Information and Communication Technologies (lCT 2013).

[3] Saman Kaedi Ebrahim Farshidi (2012), "A New Low Voltage Four-Quadrant Current Mode Multiplier", 20th Iranian Conference on Electrical Engineering, (ICEE2012), May 15-17, 2012, Tehran, Iran.

[4] Ivan Padilla-Cantoya (2012), "Compact low-voltage CMOS analog divider using a four- quadrant multiplier and biasing control circuit", 978-1-4673-2527-1/12/$31.00 ©2012 IEEE.

[5] Edson P. Santana, Raimundo Carlos S. Freire, Ana Isabela A. Cunha (2012), "A CMOS Analog Four-Quadrant Multiplier for CNN Synapses", 2012 8th International Caribbean Conference on Devices, Circuts and Systems (ICCDCS).

[6] B.Gilbert," A precise four-quadrant multiplier with sub-nanosecond response," IEEE J Solid-State Circuits, vol. SC-3,no . 4,pp. 373 1998.

[7] J.N. Badanezhad and G. C.Temes," A 20 V four quadrant CMOS analog multiplier," IEEE J. Solid-State Circuits ,1985,sc-20,pp.1158-1168.

[8] Zhenhua Wang,' A Four-Quadrant analog multiplier Using MOS Transistors Operating in the saturation Region," IEEE Trans. Instrum .Meas. vol.42, no. 1, pp.75-77, Feb.1993.

[9] M.Franciotta , G.Colli, and R. Castello," A 100-MHz 4mW Four-quadrant biCMOS Analog Multiplier," IEEE J. Solid-State Circuits, vol.32,no.10,pp.1568-1572,Oct.1997.

[10] Sho-Yuan Hsiao and Chung-Yu Wu," A 1.2 V CMOS Four-Quadrant analog multiplier," IEEE ISCAS'05 Proceedings,pp.241-244,June 1997.

[11] Boonchai boonchu and Wanlop Surakampontorn," A New NMOS Four-Quadrant analog Multiplier," IEEE ISCAS'05 proceedings, pp.1004-1007,may 2005.

[12] B.Bunchu and W.Surakampontorn "Voltage mode CMOS squarer multiplier circuit" king mongkuts institute of technology ladkrabang.

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