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Direct Single Stage Power Converter (AC/DC).

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Abstract: This study proposes a step-down tranformerless direct ac/dc converter suitable for universal line applications (90–270 V_{rms}). The topology consists of a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and both works as a step down converter. A part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Both simulation and experimental results demonstrate the validity of the proposed converter.

Keywords: AC-DC converter, Direct power transfer (DPT), integrated buck–buck–boost converter, transformerless.

1. Introduction

Now a day direct ac/dc converters have received much attention because of its cost effectiveness, compact size, and simple control mechanism. Among existing direct converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g.,≤50V), this high intermediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement. Also, in some multistage power electronics system (e.g., in data center, electrochemical and petrochemical industries, and subway applications), the isolation has been done in the PFC stage; the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, nonisolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To Protect the switch, snubber circuit is usually added resulting in more component counts. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection. To tackle the aforementioned problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported. Although the recently reported IBoBuBo converter is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters employ different PFC cells to reduce the intermediate bus voltage. Among those converters use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. In those converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in process power at least twice resulting in low power efficiency. Moreover, the reported converters consist of two active switches leading to more complicated gate control. Apart from reducing the intermediate bus voltage, the converter employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., < 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse width modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different

approaches will be given in the Section V. In this paper, an integrated buck– buck–boost converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output most common and probably it is widely used method. Capacitors, further reduction of the bus voltage can be achieved.

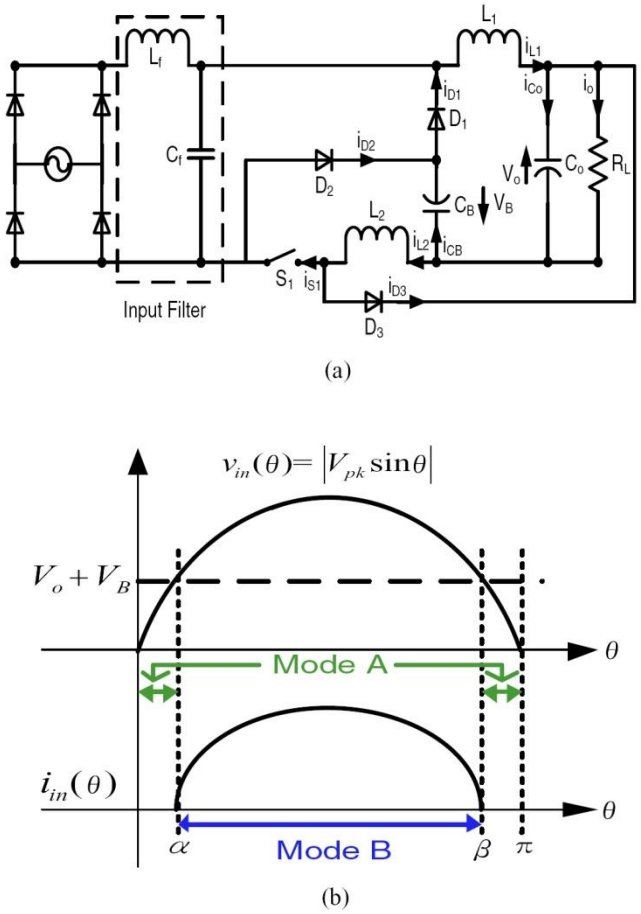


Fig. 1. (a) Proposed direct ac/dc converter.
(b) Input voltage and current waveforms

Therefore, a transformer is not needed to obtain the low output voltage. To sum up, the converter is able to achieve:

1) Low intermediate bus and output voltages in the absence of transformer;
2) Simple control structure with a single-switch;
3) Positive output voltage;
4) High conversion efficiency due to part of input power is processed once and
5) Input surge current protection because of series connection of input source and switch.

The paper is organized as follows: operation principle of the proposed IBuBuBo converter is depicted in Section II and followed by design consideration with key equations in Section III. Experimental result and discussion of the converter are given in Section IV and V, respectively. Finally, conclusion is stated in Section VI.

II. Proposed Circuit and Its Operating Principle

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and a buck–boost dc/dc cell (L_2 , S_1 , D_2 , D_3 , C_o , and C_B) is illustrated in Fig. 1(a). Although L_2 is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L_2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit. ModeA ($v_{in}(\theta) \leq V_B + V_o$):When the input voltage $v_{in}(\theta)$ is smaller than the sum of intermediate bus voltage V_B , and output voltage V_o , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage, owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f).

Fig. 3(a) shows its key current waveforms.

1) Stage 1 (period d_1T_s in Fig. 3) [see Fig. 2(a)]: When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B while diode D_2 is conducting. Output capacitor C_o delivers power to the load.
2) Stage 2 (period d_2T_s in Fig. 3) [see Fig. 2(b)]: When switch S_1 is switched OFF, diode D_3 becomes forward biased and energy stored in L_2 is released to C_o and the load.
3) Stage 3 (period d_3T_s - d_4T_s in Fig. 3) [see Fig. 2(f)]: The inductor current i_{L2} is totally discharged and only C_o sustains the load current.

Mode B ($v_{in}(\theta) > V_B + V_o$): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

1) Stage 1 (period d_1T_s in Fig. 3) [see Fig. 2(c)]: When switch S_1 is turned ON, both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($v_{in}(\theta) - V_B - V_o$), while diode D_2 is conducting.
2) Stage 2 (period d_2T_s in Fig. 3) [see Fig. 2(d)]: When switch S_1 is switched OFF, inductor current i_{L1} decreases linearly to charge C_B and C_o through diode D_1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L_2 is released to C_o and the current is supplied to the load through diode D_3. This stage ends once inductor L_2 is fully discharged.
3) Stage 3 (period d_3T_s in Fig. 3) [see Fig. 2(e)]: Inductor L_1 continues to deliver current to C_o and the load until its current reaches zero.
4) Stage 4 (period d_4T_s in Fig. 3) [see Fig. 2(f)]: Only C_o delivers all the output power.

III. Design Considerations

To simplify the circuit analysis, some assumptions are made as follows:

1) all components are ideal.
2) line input source is pure sinusoidal, i.e. $v_{in}(\theta) = V_{pk}sin(\theta)$ where V_{pk} and θ are denoted as its peak voltage and phase angle, respectively.
3) both capacitors C_B and C_o are sufficiently large such that they can be treated as constant DC voltage sources without any ripples.
4) the switching frequency f_s is much higher than the line frequency such that the rectified line input voltage $|v_{in}(\theta)|$ is constant within a switching period.

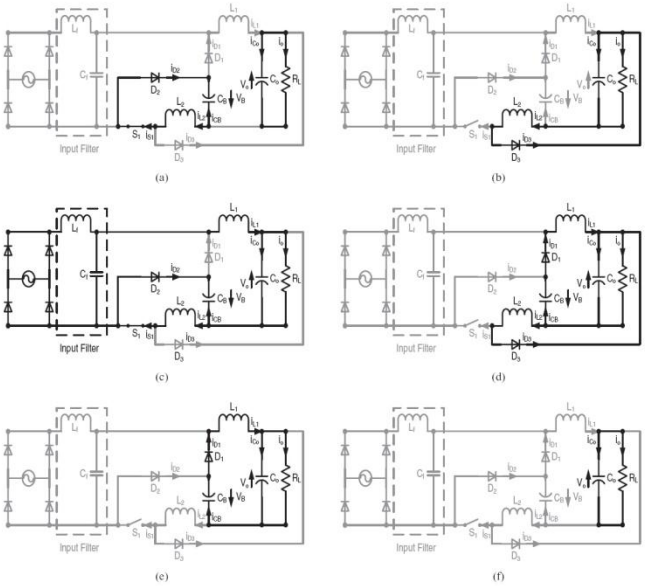


Fig. 2. Circuit operation stages of the proposed ac/dc converter.

A. Circuit Characteristics

According to Fig. 1(b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = arcsin\left(\frac{V_T}{V_{Pk}}\right)$$

$$\beta = \pi - \alpha = -\arcsin\left(\frac{V_T}{V_{Pk}}\right) \qquad (1)$$

Where V_T is the sum of V_B and V_o. Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = -2\arcsin\left(\frac{V_T}{V_{Pk}}\right) \qquad (2)$$

From the key waveforms (see Fig. 3), the peak currents of the two inductors are

$$i_{L1\,\mathrm{pk}} = \begin{cases} \dfrac{v_{\mathrm{in}}(\theta) - V_T}{L_1} d_1 T_s, & \alpha < \theta < \beta \\ 0, & otherwise \end{cases} \qquad (3)$$

And

$$I_{L2-pk} = \frac{V_B}{L_2}\, d_1 T_s \qquad (4)$$

Where T_s ($1/f_s$) is a switching period of the converter. In (3) and (4), the dependency of i_{L1} pk on θ has been omitted for clarity. It is noted that L_2 does not contribute in (3) even though it is on the current return path of the PFC cell. In addition, by considering volt–second balance of the L_1 and L_2, respectively, the important duty ratio relationships can be expressed as follows:

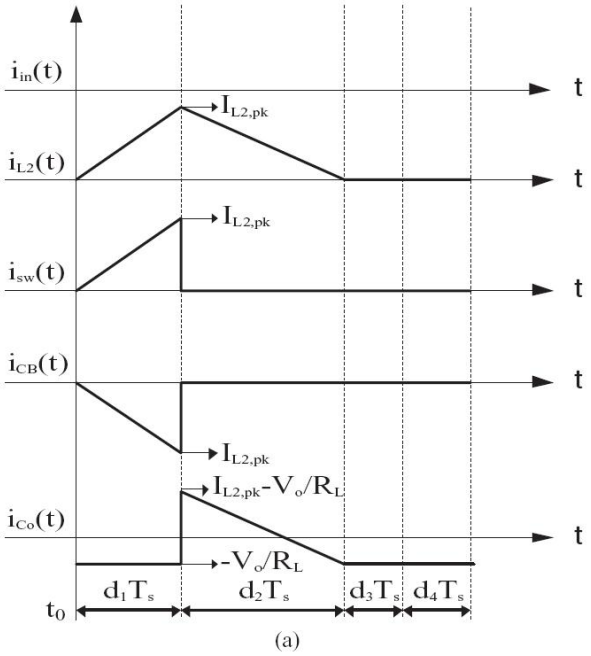
$$d_2 + d_3 = (v_{\mathrm{in}}(\theta) - V_T)/V_T d_1, \alpha < \theta < \beta$$
$$0, \text{ otherwise} \qquad (5)$$

$$d_2 = \frac{V_B}{V_o}\, d_1 \qquad (6)$$

By applying charge balance of C_B over a half-line period, the bus voltage V_B can be determined. From Fig. 3, the average current of C_B over a switching and half-line periods are expressed as follows:

$$(i_{CB})_{sw} = \frac{1}{2}\left(i_{L1\_\mathrm{pk}}(d_1 + d_2 + d_3) - I_{L2\_}\mathrm{pk}d_1\right)$$

$$= \frac{d_1^2 T_s}{2}\left\{\frac{(v_{in}(\theta) - V_T)v_{in}(\theta)}{L_1 V_T} - \frac{V_B}{L_2}\right\} \qquad (7)$$



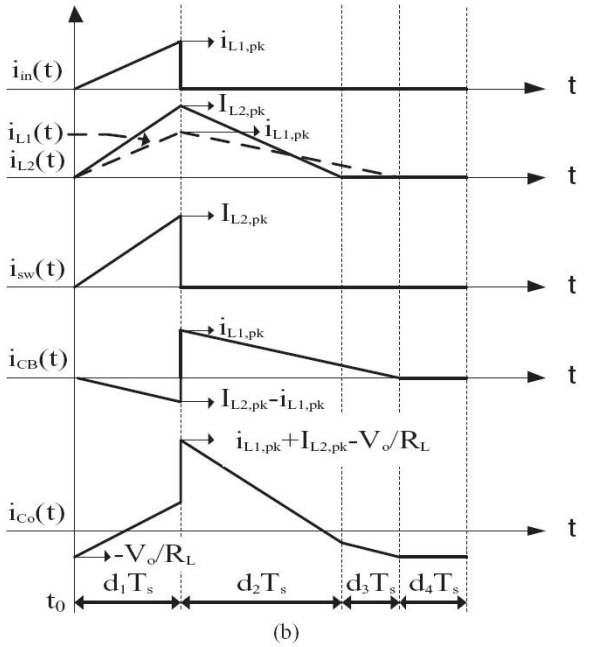


Fig.3. Key waveforms of the proposed circuit.

And

$$(i_{CB})_\pi = \frac{1}{\pi}\int_0^\pi (i_{CB})_{sw}\, d\theta$$

$$= \frac{d_1^2 T_s}{2\pi}\left[\frac{V_{pk}}{L_1}\left\{V_{pk}V_T\left(\frac{\delta}{2} + \frac{A}{4}\right)\right\} - \frac{\pi V_B}{L_2}\right] \qquad (8)$$

Where the constants A and B are

$$A = \sin(2\alpha) - \sin(2\beta) \qquad (9)$$

$$B = \cos(\alpha) - \cos(\beta) \qquad (10)$$

Putting (8) to zero due to the steady-state operation, this leads

$$V_B = \frac{MV_{pk}^2}{2\pi(V_B + V_o)}\left[\pi - 2arcsin\left(\frac{V_B + V_o}{V_{pk}}\right) - \frac{2(V_B + V_o)\sqrt{(V_{pk} + V_B + V_o)(V_{pk} - V_B - V_o)}}{V_{pk}^2}\right]$$

Where M is the inductance ratio L_2/L_1. As observed from (11), the bus voltage V_B can be obtained easily by numerical method. It is noted that V_B is independent on the load, but dependent on the inductance ratio M. Fig. 4 depicts the relationship among V_B, rms value of the line voltage, and inductance ratio M. It is noted that the bus voltage is kept below 150 V at high-line input condition.

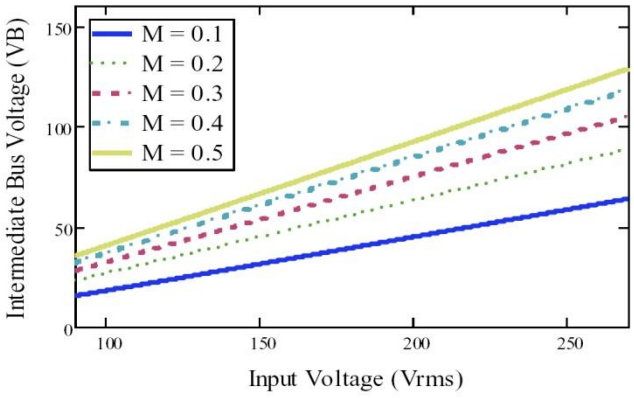


Fig. 4. Calculated intermediate bus voltage under different inductance ratios.

The rms value of the input current, average input power and power factor are given by

$$p.f = \frac{\frac{1}{2}\int_{\alpha}^{\beta} v_{in}(\theta)\,(i_{in})d\theta}{\frac{V_{pk}}{\sqrt{2}} I_{in\_rms}}$$

$$= \frac{V_{pk}\left(\frac{\gamma}{2} + \frac{A}{4}\right) - V_T B}{\sqrt{V_{pk}^2\left(\frac{\gamma}{2} + \frac{A}{4}\right) - 2V_{pk}V_T B + \gamma V_T^2}} \sqrt{\frac{2}{\pi}} \quad \text{—(12)}$$

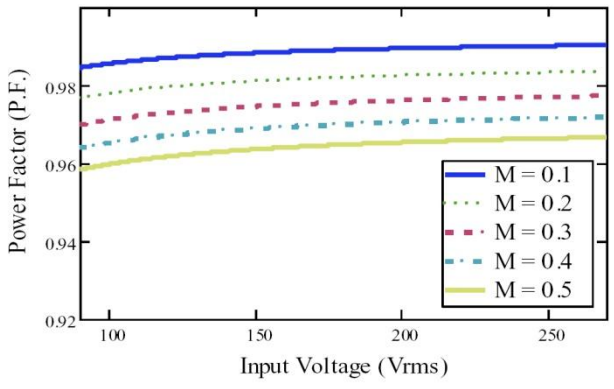


Fig. 5. Estimated power factor under variation of inductance ratios.

IV. SIMULATION RESULTS

The performance of the proposed circuit is verified by the Matlab simulation. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power (> 97%), the inductance ratio has to be optimized according to Figs. 4 and 5. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used.

CIRCUIT COMPONENTS

Parameters	Values
IC Controller	TL594
Input filter inductor L_f	2 mH
Input filter capacitor C_f	2 µF
Inductor L_1	109 µH
Inductor L_2	48 µH
Inductance Ratio	(M = L_2/L_1) 0.440
MOSFET S_1	SPW47N60CFD
D_1	MUR3040PT
D_2	MUR3040PT
D_3	MUR3040PT
C_B	7 mF
C_o	7 mF

In addition, the inductance ratio will affect the efficiency of the converter. More detail will be given in Section V. Taking the performance of the converter on bus voltage, power factor, and efficiency into account, the inductance ratio around M = 0.4 is selected. Table II depicts all the components used in the circuit, and its specification is stated as follows:

1) output power: 100 W
2) output voltage: 19 V_{dc}
3) power factor: > 96%
4) intermediate bus voltage: < 150V
5) line input voltage: 90–270 V_{rms}/50 Hz
6) switching frequency (f_s): 20 kHz

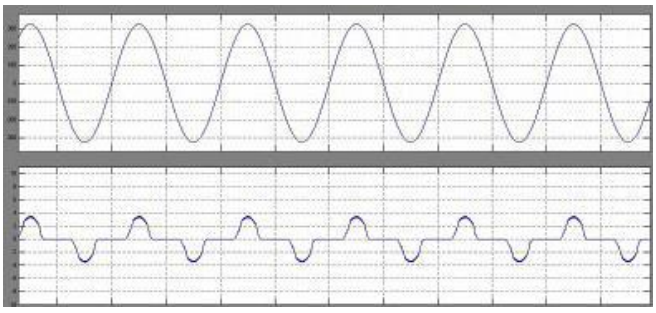


Fig. 7. Measured input characteristic of the converter at 270 Vrms under 120-W condition.

Fig. 7 shows the waveforms of the line-input voltage along with its current under full load condition at 270 V_{rms}. Fig. 8. In addition, is the simulation circuit and Fig. 9 is the measured output voltage at 270 V_{rms} under full load condition. It can be seen that the bus voltage was kept at 123 V and well below 150 V at high line condition. Fig. 10 illustrates the conversion efficiency of the proposed converter under different line input and output power conditions. The maximum efficiency of the circuit is around 89% at low line application. Furthermore, Fig. 11 shows the Transient response between 40% and 100% of load.

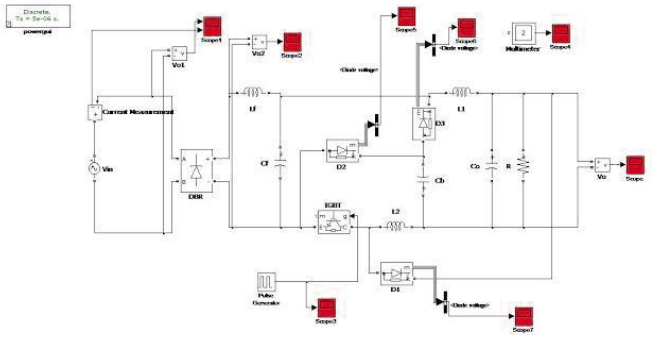


Fig. 8. Simulation circuit

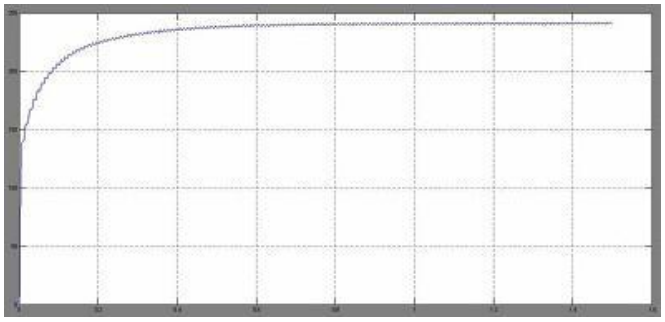


Fig. 9. Measured output voltage bus voltage at 270 V_{rms} under full load Condition

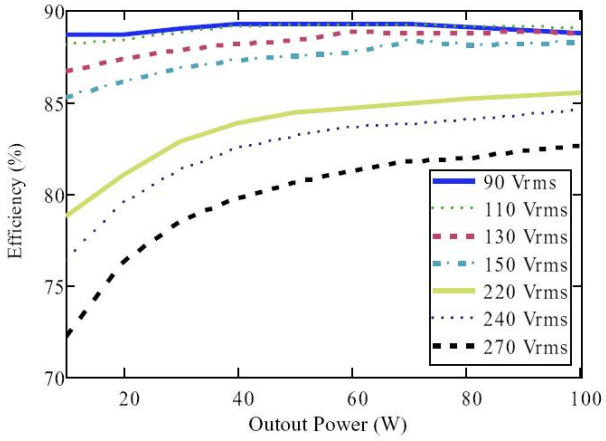


Fig. 10. Measured circuit efficiency under load variation.

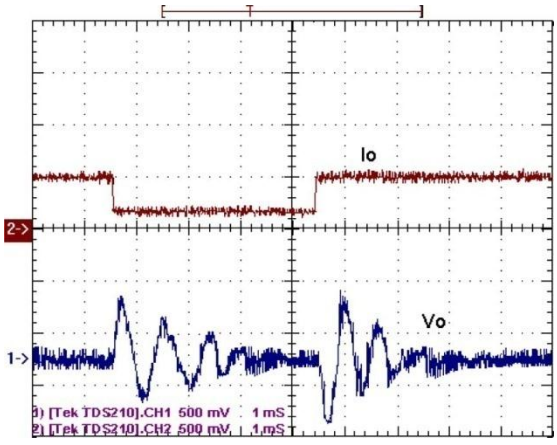


Fig. 11. Transient response between 40% and 100% of load. Upper: output current I ; lower: output voltage V.

VI. CONVERTER OPERATION PRINCIPLE

The proposed converter shown in Fig. 1 is analyzed with six assumptions in this section.

1) Input voltage v_{ac} is considered to be an ideal rectified sine wave, i.e., $v_i = V_m \mid \sin(\omega_L t)\mid$, where V_m is the peak amplitude and ω_L is the line angular frequency.
2) All components are ideal; thus, the efficiency is 100%.
3) Switching frequency f_s is much higher than ac line frequency f_L , so that the input voltage can be considered constant during one switching period T_s .
4) Capacitor C is big enough such that voltage V_C can be considered constant during T_s . Furthermore, output voltage V_o is pure dc without twice the line frequency ripple.
5) Both inductors L_1 and L_2 operate in the DCM. Further- more, the current in inductor L_1 (i_{L1}) reaches zero level prior to the current in L_2 (i_{L2}).
6) The phase shift of the input line current introduced by the input filter is minimal and can be neglected. With these assumptions, the circuit operation over one switching period T_s can be described in three operating stages, as shown in Fig. 12

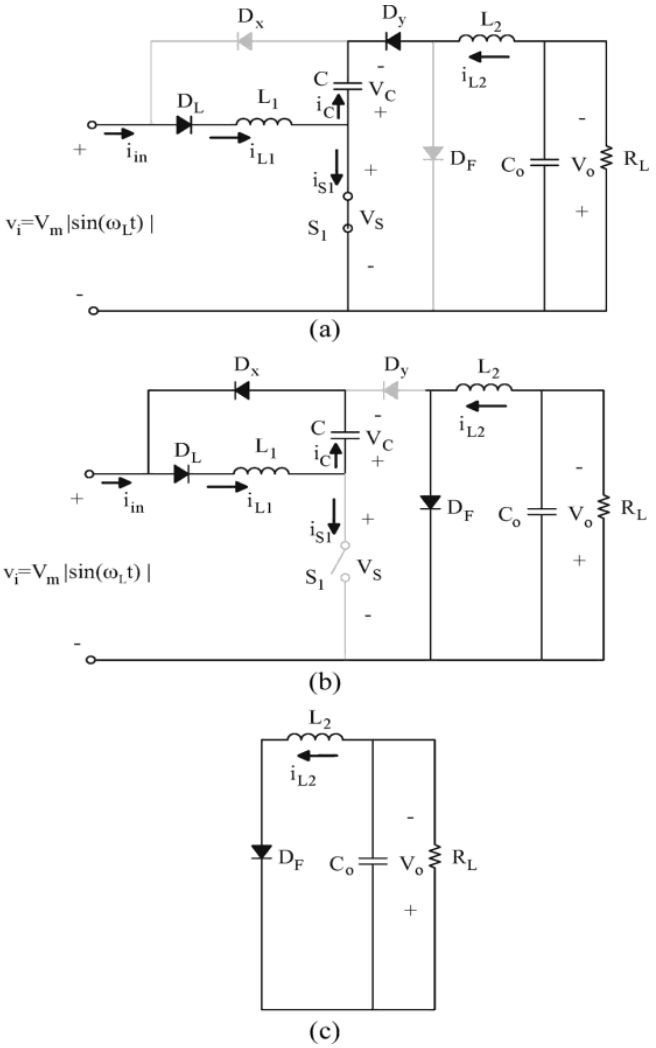


Fig.12. Operating stages of the proposed converter. (a) Stage 1. (b)Stage 2. (c)Stage 3.

Stage 1 **[t_0 , t_1]*:*** Prior to this interval, the currents through L_1 and L_2 are at ground level. When switch S_1 is turned on at $t = 0$, diode D_y becomes forward biased, and currents i_{L1} and i_{L2} begin to linearly increase. This interval ends when switch S_1 is turned off, initiating the next stage.

Stage 2 **[t_1 , t_2]:** When the switch is turned off, diode D_y becomes reverse biased. Thus, current i_{L1} linearly decreases through diode D_x , whereas current i_{L2} linearly decreases at a rate proportional to output voltage V_o through the freewheeling

diode D_F . This stage ends when current i_{L1} reaches the ground level. Diode D_L prevents current i_{L1} from becoming negative. ***Stage 3*** **[t_2 , t_3]:** In this stage, current i_{L2} continues to de- crease through the freewheeling diode D_F until it becomes zero. The converter stays in this stage until the switch is turned on again. To improve the overall efficiency, it is preferred to turn on the switch at $t = t_3$, which will reduce the current stresses through the semiconductor devices. The characteristic ideal circuit waveforms during one switching period are shown in Fig.13

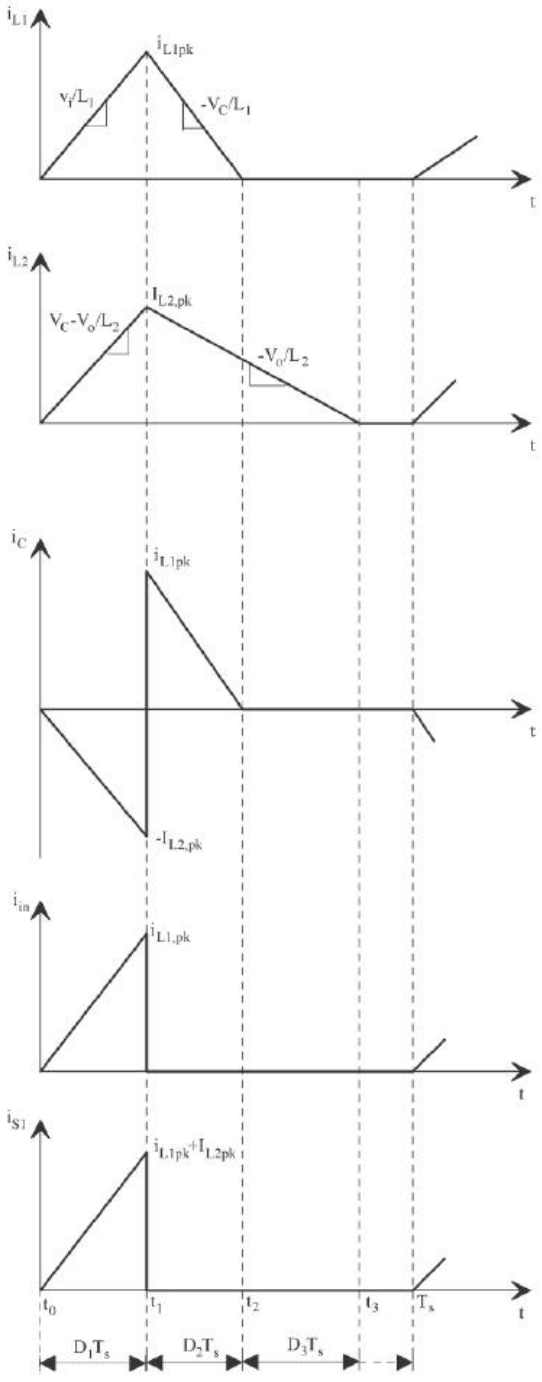


Fig.13. Characteristic waveform of ideal circuit on switching period.

V. DISCUSSION

According to direct power transfer ratio n under this type of capacitive coupling is V_o/V_T . It can be seen that the portion of direct power transfer from input to output decreases when VB becomes larger resulting in increase of VT . In other words, the direct power transfer decreases when the line input voltage increases. It matches with the discussion in Section III-E. In addition, the increase of VB will lower the conversion efficiency of dc/dc cell due to larger voltage conversion around ten times at high-line condition, from VB = 123 V down to Vo = 19 V. As a result, it further impairs the efficiency of the converter at high-line operation. On the other hand, from (2), decrease of VB extends the conduction angle of the converter leading to higher power factor. However, lower VB requires decrease of inductance ratio resulting in higher peak inductor currents and causing higher conduction loss. Thus, tradeoff has to be made for selecting the inductance ratio among the peak current of inductors, bus voltage, and power factor. Nevertheless, the converter is capable to be used under high-line condition with the full load efficiency around 84% at 240 Vrms .

VI. CONCLUSION

The proposed direct ac/dc converter has been simulated, and the results have shown in good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below150Vat all input and output conditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. The absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance and the cost of the proposed circuit are reduced compared with the isolated counterparts.

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