www.ijecs.in
International Journal Of Engineering And Computer Science ISSN:2319-7242
Volume - 3 Issue -9 *September*, 2014 Page No. 8123-8128

Design & Implementation of Binary Phase Shift Keying Demodulation through phase locked loop

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Abstract: ***This paper describes about BPSK demodulation using costas loop and implementing on a DSP kit. The demodulation process can be divided into three major subsections. First, since the incoming waveform is suppressed carrier in nature, coherent detection is required. The methods by which a phase-coherent carrier is derived from the incoming signal are termed carrier recovery. Next, the raw data are obtained by coherent multiplication, and used to derive clock-synchronization information. The raw data are then passed through the filter, which shapes the pulse train so as to minimize inter symbol-interference distortion effects. This shaped pulse train is then routed, along with the derived clock, to the data sampler which outputs the demodulated data. The codes for the PLL and the Costas loop are written in C language and implemented on the DSP kit ADSP 21060 [4,5]. The various input and output plots are observed on the SHARC (Super Harward Architecture) simulator and also on the Emulator.***

Keywords: BPSK demodulation, Phase locked loop, Costas loop.

1. Introduction

In the earlier days in satellite communication analog systems were used for the communication between the base station and the satellite, but there were many disadvantages of using the analog systems for satellite communication. The incorporation of the analog system for communication occupied large area on the satellite up to few square feet. This would in turn lead to more consumption of the fuel which was not preferred. This lead to the use of digital systems for communication [6].

The advantages of the digital systems are, they are less expensive, more compatible, easy to manipulate, flexible, compatible with other digital systems, transmission without degradation and integral network. These advantages lead to use of digital systems in satellite communication.

There are different techniques of digital modulation namely ASK (Amplitude shift keying), FSK (frequency shift keying), PSK (phase shift keying), QPSK (quadrature phase shift keying), MSK (minimum shift keying), but for satellite communication the BPSK is employed the reason behind that is communication between the base station and the satellite is small commands in which the data rate is less of around 4Kbps , hence the BPSK type of modulation and demodulation is employed. BPSK is preferred over FSK because FSK causes Doppler shift, it uses high speed transmission and less efficient in both power and bandwidth.[7,8].

2. Phase – Locked Loops

The Phase-locked Loop (PLL) is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. Many research efforts have been made on clock recovery circuits (CRC), and phase locked loops have been considered desirable for monolithic implementation of CRC [1].

A PLL is a circuit, which causes a particular system to track with another one. More precisely a PLL is a circuit synchronising an output signal(generated by an oscillator) with a reference or input signal in frequency as well as in phase. In the synchronized- often called locked –state the phase error between the oscillator's output signal and the reference signal is zero, or remains constant. A PLL is a feedback system containing three basic components:

- Phase Detector
- Loop Filter
- Voltage Controlled Oscillator

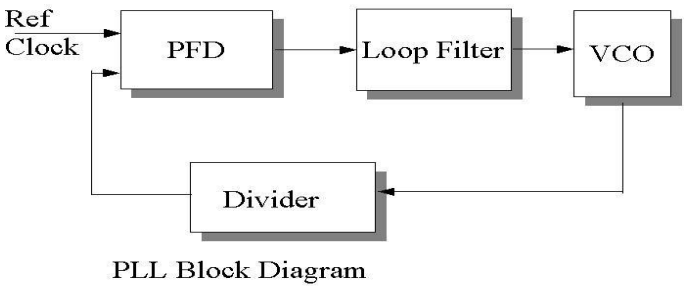


Figure 1: Phase Locked Loop Block Diagram

3. OPERATION OF A BASIC PLL

In order to understand the basic operation of a PLL, it is important to know the various signals associated with it,

- The reference (or input) signal $U_1(t)$
- The angular frequency ω_1 of the reference signal
- The output signal $U_2(t)$ of the VCO
- The angular frequency ω_2 of the output signal
- The output signal $U_d(t)$ of the phase detector
- The output signal $U_f(t)$ of the loop filter
- The phase error θ_e defined as the phase difference between the signals

Let us now look at the operation of the three basic blocks in a PLL

3.1 Voltage Controlled Oscillator (VCO)

The VCO is an oscillator that produces a periodic waveform, the frequency of which depends on the applied input voltage. The free running frequency, is the frequency of the VCO output when the applied input is zero.

The angular frequency is given by

$$\omega_2(t) = \omega_0 + K_0 U_f(t) \qquad (1)$$

Where, ω_2 is the center (angular) frequency of the VCO and k0 is the VCO gain in $s^{-1}V^{-1}$.

3.2 Phase detector

The phase detector (PD) compares the phase difference between the input data and recovered clock and creates an error signal to signal to drive the frequency and the phase of the VCO to lock. The PD produces an output signal that is a function of the phase difference between of the incoming signal and the oscillator signal. Many Parameters of the PLL, such as the phase output, loop gains and the jitter performance depend on the properties of the phase detector. So the choice of the phase detector is one of the key design issues.[2]

The PD is also referred to as the phase comparator develops an output signal which is approximately proportional to the phase error θ_e,

$U_d(t) = K_d \theta_e \qquad (2)$

Here K_d represents gain of the PD. The output signal of the PD consists of a dc component and superimposed ac components. The latter is undesired hence it is cancelled by a loop filter. In most cases a first order filter is used.

3.3 Low Pass Filter

The Low Pass Filter blocks high frequencies out of the incoming signal from the phase detector. The filter is represented by its transfer function which is determined by the loop parameters, gain of the VCO and gain of the phase detector. The filtered signal is the control signal that is used to change the frequency of the VCO Output.

Working: First we assume that the angular frequency of the input signal is equal to the center frequency. The VCO then operates at its center frequency, at this stage the phase error will be zero. If is zero, the output signal of the PD will also be zero consequently the output signal of the loop filter will be zero. This condition permits the VCO to operate at its center frequency. If the phase error were not zero initially, the PD would be develop a non-zero output. After some delay the loop filter will produce a finite signal.[3] This would cause the VCO to change its center frequency in such a way that the phase error finally vanishes.

Assume that the frequency of the input signal is changed suddenly at time t_0, by an amount. Then the phase of the input signal starts leading the phase of the output signal. A phase error is built up and increases with time. The PD develops a signal which also increases with time. With a delay given by the loop filter, will also rise. This causes the VCO to increase its frequency. This phase error θ_e becomes smaller now, and after some settling time the VCO will oscillate at a frequency that is exactly the frequency of the input signal. Depending on the type of loop filter used, the final phase error will have reduced to zero or to a finite value.[11] .The VCO now operates at a frequency which is greater then its center frequency by an amount $\Delta\omega$. This will force the signal to settle at a final value of $U_f(t) = \frac{\Delta\omega}{k_0}$.

If the center frequency of the input signal is frequency modulated by an arbitrary low frequency signal, then the output signal of the loop filter is the demodulated signal. The PLL can consequently be used as an FM detector. One of the most important capabilities of the PLL is its ability to suppress noise superimposed on its input signal. If in case the input signal of the PLL is buried in noise, the PD tries to measure the phase error between input and output signals. The noise at the causes zero crossings of the input signal to be advanced or delayed in a stochastic manner.

This causes the PD output signal to jitter around an average value. If the corner frequency of the loop filter is low enough, almost no noise will be noticeable in the signal and the VCO will operate in such a way that the phase of the signal is equal to the average phase of the input signal that is buried in noise. These implications show that the PLL acts as a servo system which controls the phase of the output signal.

4. Various States in a PLL

If begins to increase, the phase comparator output will be positive which in turn increases the frequency of the VCO. A new equilibrium point will be reached when the frequency of the input signal and the frequency of the VCO output will be identical, thus PLL starts tracking the input signal and when it does so, it is said to be in "locked state". If the applied signal has an initial frequency of, the PLL will acquire lock and the VCO will track the input signal frequency over some range, provided that the input frequency over some range, provided that the input frequently chances slowly. However the loop will remain locked over some finite range of the frequency shift. This range is called the Hold-in (or lock) range. The hold-in range depends on the overall dc gain of the loop, which includes the dc gain of the LPF.

On the other hand, if the applied signal has an initial frequency not equal to, the loop may not acquire lock even though the input frequency is within the hold-in range. The frequency range over which the applied input will cause the loop to lock is called the pull-in (or capture) range. This range is primarily determined by the loop filter characteristics, and it is never greater than the hold-in range. Another important PLL specification is the maximum locked sweep rate. It is defined

as the maximum rate of change of the input frequency for which the loop will remain locked. If the input frequency changes faster than this rate, the loop will drop out of lock.[12]

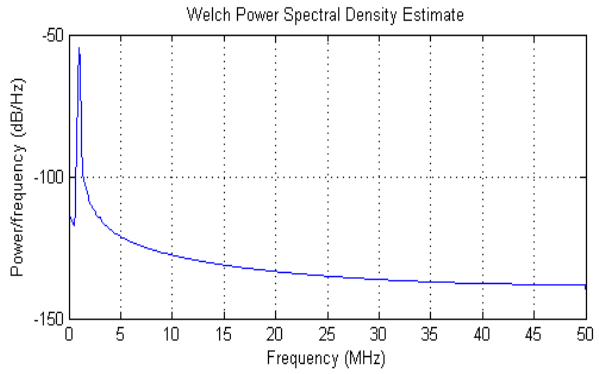


Figure 2 : Power spectral density estimate

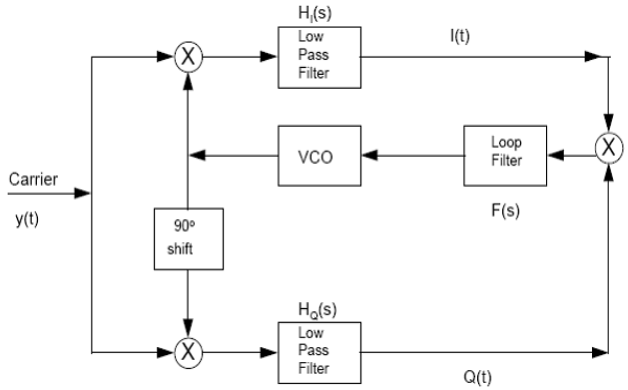
A typical lock-in characteristics is shown above. The solid curve shows the VCO control signal as the sinusoidal testing signal swept from a low frequency to a high frequency (with the free-running frequency of the VCO, being within the swept band). The dashed curve shows the result when sweeping from high to low. The hold-in range is related to the dc gain of the PLL by

$$\Delta f_h = \frac{K_v K_d F(0)}{2\pi} \qquad (3)$$

5. Costas Phase Locked Loop

The costas loop can be used as a demodulator circuit used to demodulate the binary data from its carrier sine wave. The costas PLL is analyzed by assuming that the VCO is locked to the input suppressed carrier frequency, f_c with a constant phase error .

Then the voltages v(t) and $U_f(t)$ are obtained at the output of the baseband low pass filter. Since is small, the amplitude of v(t) is relatively large compared to that of the $U_f(t)$. Aso $v_1(t)$ is proportional to m(t), so it is demodulated output.



$$s(t) = A_c m(t)\cos\omega_c t \qquad (4)$$

$$v_4(t) = K\sin 2\theta_e \qquad (5)$$

The Product voltage $v_3(t)$ is

$$v_3(t) = \frac{\left(\frac{A_0 A_c}{2}\right)^2 m^2(t)\sin(2\theta_e)}{2} \qquad (6)$$

The voltage $v_3(t)$ is filtered with a low pass filter that has a cutoff frequency near DC so that this filter acts as an integrator to produce the DC VCO control voltage.

$$v_4(t) = K\sin(2\theta_e) \qquad (7)$$

Where, $K = \frac{\left(\frac{A_0 A_c}{2}\right)^2 m^2(t)}{2}$

The DC control voltage is sufficient to keep the VCO locked to f_c with a small phase error θ_e.

6. The Linear PLL(LPLL)

Analog PLL's are generally known as the linear PLLs. A LPLL is a basic PLL from which the other PLLs are derived. By understanding the working of a LPLL, it is easy to design software PLLs based on LPLL design equations.

If we assume that LPLL has locked and stays locked for the next future, we can develop a linear mathematical model for the system. The mathematical model is used to calculate a phase-transfer function H(s) which relates the phase θ_1 of the input signal to the phase θ_2 of the output signal.

$$H(s) = \frac{\Theta_2(s)}{\Theta_1(s)} \qquad (8)$$

Where, $\Theta_2(s)$ and $\Theta_1(s)$ are the Laplace transforms of the phase signals $\theta_1(t)$ and $\theta_2(t)$ respectively. H(s) is called the phase transfer function. To get an expression of H(s) we need to derive the transfer functions for the individual blocks.

Since the input for the LPLL is a sine wave, we can write,

$$u_1(t) = U_{10}\sin(\omega_1 t + \theta_1) \qquad (9)$$

Assuming that the output of VCO is a square wave we have,

$$u_2(t) = U_{20}\sin(\omega_2 t + \theta_2) \qquad (10)$$

From the figure 4 we can observe that, the dashed curve in a sine wave having a phase θ_1=0 , the solid line has a non-zero phase θ_1. Let us assume that the phase is constant over time. The dashed curve in fig b shows a symmetrical Walsh function W(ω_2t) having a phase θ_2= 0, the solid line has a non-zero phase. The output signal of the 4 quadrant multiplier is obtained by multiplying the signals u_1 and u_2.

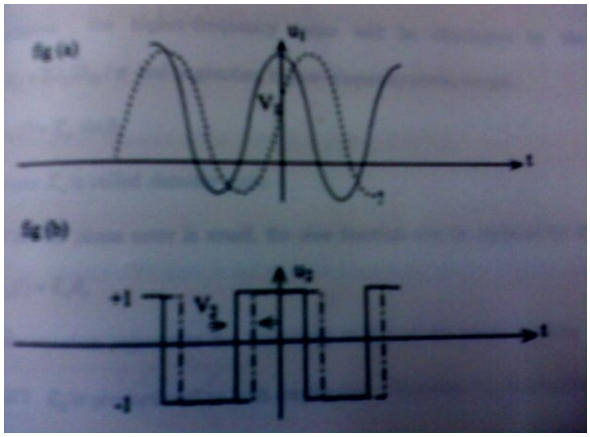


Figure 4: PLL output

The Walsh function is replaced by it's Fourier series we get

$$u_2(t) = U_{20}\left\{\frac{4\cos(\omega_2 t+\theta_2)}{\pi}+\frac{4\cos(3\omega_2 t+\theta_2)}{3\pi}+\cdots\right\} \quad (11)$$

The first term in the flower brackets is the fundamental component, the remaining terms are odd harmonics.

We have,

$$u_d(t) = u_1(t)u_2(t) = U_{10}U_{20}\sin(\omega_1 t+\theta_1)\times\left\{\frac{4\cos(\omega_2 t+\theta_2)}{\pi}+\frac{4\cos(3\omega_2 t+\theta_2)}{3\pi}+\cdots\right\} \quad (12)$$

When the LPLL is locked, the frequency ω_1 and ω_2 are identical and $u_d(t)$ becomes,

$$u_d(t) = U_{10}U_{20}\left[\frac{2\sin\theta_e}{\pi}+\cdots\right] \quad (13)$$

Where $\theta_e = \theta_1 - \theta_2$ is the phase error.

The first term in this series is the wanted "DC term", whereas the higher frequency terms will be eliminated by the loop filter.

Taking $K_d = 2\frac{U_{10}U_{20}}{\pi}$ and neglecting high frequency terms we get,

$$u_d(t) \approx K_d\sin\theta_e \quad (14)$$

Where K_d is called detector gain

When the phase error is small, the sine function can be replaced by its argument, and we have

$$u_d(t) \approx K_d\theta_e \quad (15)$$

This equation represents the linearized model of the phase detector. The dimension of K_d is rad/volt. K_d is proportional to both amplitudes. Normally U_{20} is a constant, so K_d becomes a linear function of the input signal level U_{10}. Therefore it can be said that, in the locked state of the LPLL, the phase detector represents a zero order block having a gain of K_d.

Let us now derive the transfer function of the VCO. The angular frequency of the VCO is given by

$$\omega_2(t) = \omega_0 + \Delta\omega_2(t) = \omega_0 + K_0\omega_2(t) \quad (16)$$

Where K_0 is called the VCO gain.

The model of the VCO should yield the output phase θ_2. By definition, the phase θ_2 is given by the integral over the frequency variation $\Delta\omega_2$.

$$\theta_2(t) = \int \Delta\omega_2\, dt = K_0\int u_f\, dt \quad (17)$$

In the Laplace transform, Integration over the time corresponds to division by s, so the Laplace transform of the output phase θ_2 is given by

$$\Theta_2(s) = \frac{K_0 U_f(s)}{s} \quad (18)$$

The transfer function of the VCO is given by,

$$\frac{\Theta_2(s)}{U_f(s)} = \frac{K_0}{s} \quad (19)$$

If we consider a PI filter as the loop filter, then we have the phase transfer function as

$$H(s) = \frac{\frac{K_0K_d(1+s\tau_2)}{\tau_1}}{s^2+\frac{sK_0K_d\tau_2}{\tau_1}+\frac{K_0K_d}{\tau_1+\tau_2}} \quad (20)$$

If we substitute

$$\omega_n = \sqrt{\frac{K_dK_0}{\tau_1}}$$

And $$\zeta = \frac{\omega_n\tau_2}{2} \quad (21)$$

Where ω_n is the natural frequency and ζ is the damping factor

We have,

$$H(s) = \frac{2s\zeta\,\omega_n+\omega_n^2}{s^2+2s\zeta\,\omega_n+\omega_n^2} \quad (22)$$

The term K_dK_0 is called the Loop gain.

If $K_dK_0 = \omega_n$, then the LPLL system is said to be a high gain loop, otherwise it is called a low gain loop. Most practical LPLLs are high gain loops.

7. Implementation of Phase Locked Loop

The PLL makes use of a Multiplier as a phase detector, an IIR Low Pass Elliptical Filter, a PI loop filter and an integrator as a VCO. For a periodic signal, its frequency in Hz is equal to the rate of change of phase in 2Π segments, or conversely, phase is the integral of the frequency over a certain period of time. Thus a VCO can be replaced an integrator. For the purpose of easy simulation, a low frequency waveform such as 3Hz is given as the input. Therefore the integrator is initially given a value of 3Hz which is its central frequency. The cosine of the integrator output is given as a feedback and the sine of the integrator output is taken as the output.[10]

Algorithm

- Get sampled input $y_i(n)$
- Multiply input $y_i(n)$ with the feedback $y\phi(n)$
- Pass $y\phi(n)$ through a low pass filter, given by the equation,

$$\omega(n) = \omega(n-1)c1 - \omega(n-2)c2 + y\phi(n)c3 - y\phi(n-1$$

Where n-1 refers to the past value and n-2 to the one before that.

c1-c5 are co-efficient that determine the cut off frequency of the filter.

- Pass $\omega(n)$ through a PI filter given by the equation

$a1(n)=a1(n-1)+K_p\ \omega(n)-K_p\ \omega(n-1)+\frac{K_1 T_s \omega(n)}{2}+\frac{K_1 T_s \omega(n-1)}{2}$

where K_p and K_1 refer to the product and integrator constants respectively.

- a1(n) is then passed through an integrator given by the equation

$$y_m(n)=\frac{a_1(n)T_s}{2}+\frac{a_1(n-1)T_s}{2}+y_m(n-1)$$

where T_s is the time period of the signal.

- The cosine of the integrator output y_0 is given as the feedback and the sine output y_1 given to the output.

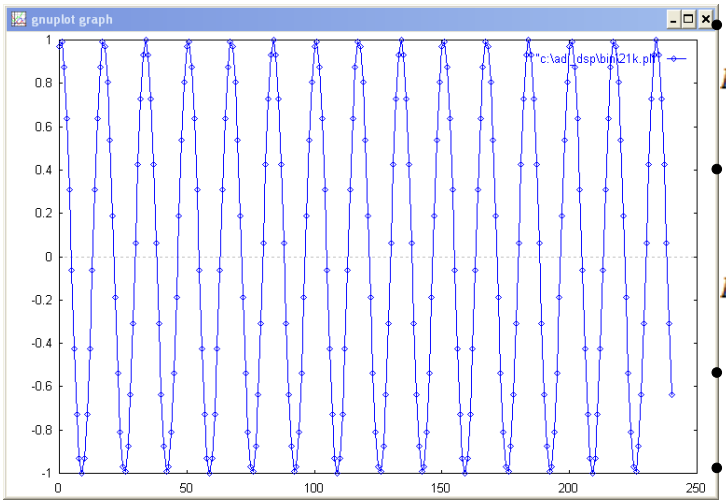


Figure 5: PLL input waveform,3Hz

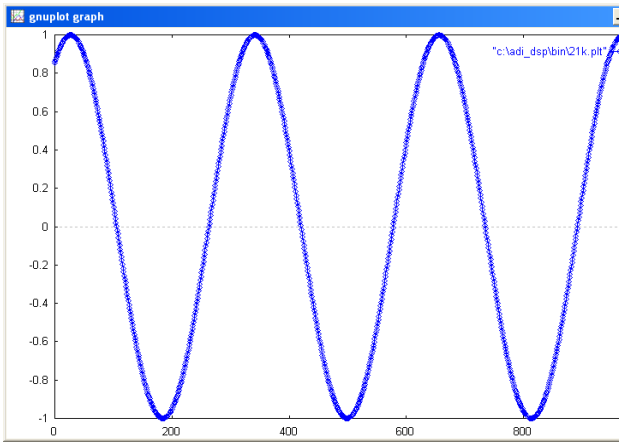


Figure 6: PLL output waveform

8. Implementation of Costas Loop

A costas loop can be created by making use of 2 PLLs wherein 1 PLL is 90^0 phase shifted from the other. Some small modifications have been made to the PLL block mentioned before to achieve better performance for the costas demodulation section.

Algorithm

- Attain s(n), the input sample multiply it with SI_2 to form s_1 and multiply s(n) with CI_2 to form s_2.
- Output of the low pass filter $f_1(n)$ is given by

$f_1(n)= f_1(n-1)c_1 - f_1(n-2)\ c_2 + s_1(n)c_3 - s_1(n-1)c_4 + s_1(n-2)c_5$.

Output of the low pass filter

$f_2(n)= f_2(n-1)\ c_1 - f_2(n-2)\ c_2 + s_2(n)c_3 - s_2(n-1)c_4 + s_2(n-2)c_5$

where n-1 refers to the past value and n-2 refers to the one before that . (c_1 to c_5) are the coefficients that are determine the cutoff frequency of the filter.

- Output of the low pass filter $f_1(n)$ is taken as the output and simultaneously multiplied with the $f_2(n)$ to form $M_1(n)$.
- $M_1(n)$ is passed through an integrator having an equation

$$I_1(n)=\frac{m_1(n)t_s}{2}+\frac{m_1(n-1)t_s}{2}+I_1(n-1)$$

- A_d is then multiplied with a gain of 2 to form and then passed on to an integrator, given by the equation.

$$I_1(n)=\frac{G3(n)ts}{2}+\frac{G3(n-1)ts}{2}+I_2(n-1)$$

- The sine of $I_2(n)$ is given by the multiplier 1 and cosine of $I_2(n)$ is given to multiplier 2.
- The past and present values are updated, i.e n is given to n-1 and n-1 is given to n-2.
- The whole process is repeated until the last sample is received.

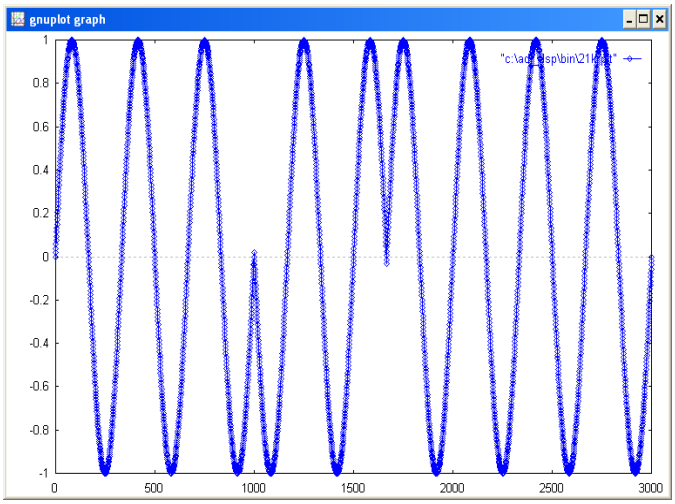


Figure 7: Input Modulated waveform(frequency 3Hz)

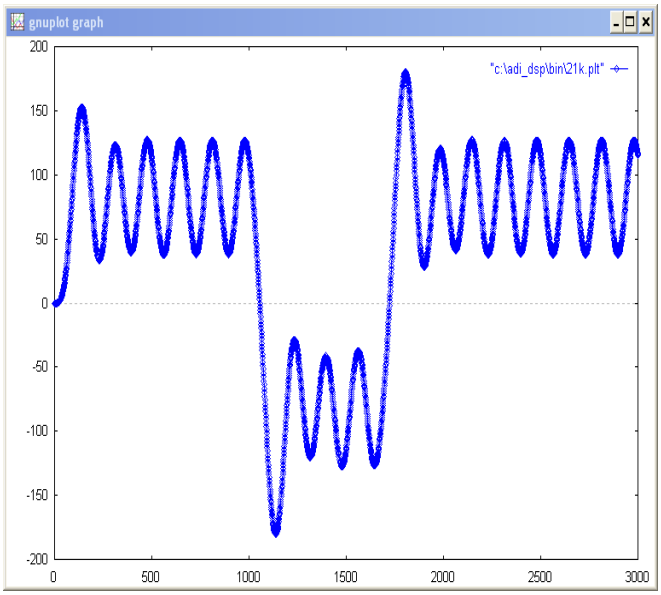


Figure 8: Output Demodulated waveform

9. Conclusion

A lot of thought, research and experimentation has gone into this project. There is no such thing as an ideal design, further modifications can be done to this project to improve its performance. For any assignment a basic foundation is necessary and this is what we have tried to achieve in this venture. Costas demodulation loop has been successfully implemented using ADSP 21062 processor. By making slight modifications of the design equations it is possible to use the same program for real time high quality demodulation purpose. The focus of this project does not lie in merely implementing some concept, but rather in studying the various ways in which it can be implemented.

10. Future Scope of the Project

BPSK modulation and demodulation is used for a low data transmission of commands from the base station to the satellite system. Also there is sometimes phase ambiguity at the receiver. So for transmitting any information at a higher data rate and in order to improve the overall efficiency, it can be extended to Quadrature Phase Shift Keying (QPSK) in which two bits can be represented using a single phase of the carrier. The error rates of both BPSK and QPSK are same. In QPSK the bandwidth requirement is half as that of BPSK and data rate is twice. Also this can be extended to M-array modulation in which M bits are represented using one phase of the carrier thus reducing the bandwidth requirement.

References

[1] Roland E. Best- Phase Locked Loops- Design, Simulation, and Applications *McGraw-Hill 1999.*

[2] Paul V. Brennan Phase-Locked Loops- Principles and Practice *Macmillan Press Ltd 1996.*

[3] Alain Blanchard-Phase-Locked Loops-Applications to Coherent Receiver Design *John Wiley & Sons Inc. 1976.*

[4] Hari Krishna Garg-Digital Signal Processing Algorithms *CRC Press LLC. 1998.*

[5] Johnathan(Y) Stein-Digital Signal Processing –A computer Science Perspective *A Wiely Interscience Publictions 2000.*

[6] JJ Spilker-Digital Communications by Satellite *Prentice Hall Inc. 1977.*

[7] Leon W. Couch. Digital and Analog Communication systems *Prentice Hall Inc. 1977.*

[8] Benjamin C. Kuo- Automatic Control Systems *Prentice Hall Inc. 1995.*

[9] ADSP 21000 Family Assembler Tools and Simulator Manual- July 1995.

[10] Santanu Sarma, P.K. Maharana and V.K. Agarwal – Flexible Mode Frequency Trackling using Phase Locked Loop July 2004.

[11] Marcelo J. Bruno, Juan E. Cousseau and Pedro D. Donate on reduced complexity Iir Adaptive filters (2005 IEEE International Symposium on circuits and systems)

[12] William Stallings- Wireless Communication and Networking *Pearson Education Inc. 2005.*

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