

CMOS Digital Based Technology for Static Power Reduction in Nanoscale Circuits

Srivivas kolli

Abstract:

In this paper an overview on the main issues in analog IC design in scaled CMOS technology is presented. Decreasing the length of MOS channel and the gate oxide has led to undoubted advantages in terms of chip area, speed and power consumption (mainly exploited in the digital parts). Besides, some drawbacks are introduced in term of power leakage and reliability. Moreover, the scaled technology lower supply voltage requirement has led analog designers to find new circuitual solution to guarantee the required performance. Power gating with high-K transistors is then investigated to analyze the effects of such a combination. Finally, the results are compared and the effectiveness of the various leakage reduction techniques is analyzed. Threshold voltage change proved to have the most impact on performance and less of an impact on leakage reduction while power gating offered no significant performance drop and the highest impact on leakage power reduction.

Index Terms—CMOS inverter, cadence, static power, sleepy keeper, threshold voltage, transistor stacking

1 Introduction

Technology scaling and the large number of transistors on an integrated circuit has resulted in several design challenges, including increased leakage power, increased wire capacitance, increased resistance due to temperature, and an increase in soft error rate [1]. As technology progresses and allows for smaller feature sizes, the nature of power consumption in CMOS circuits changes. Smaller channel lengths and supply voltages ultimately reduce dynamic power consumption per transistor and permit faster transistor operation. While desirable, transistor scaling also comes with a drawback; the smaller gate oxide thickness and the lower threshold voltage substantially increase the transistor leakage power consumption. As a result, as transistors become smaller and smaller, the leakage power consumption grows and is now a significant problem that has to be addressed [2].

The power is emerging as the most critical and vital issues in system on chip design today and management of power in every category of design is becoming an increasingly urgent problem. In early 1970's, providing high speed operation with minimum area were main aim of design. Many design tools are concentrated to achieve these goals.

A. Power Reduction

In digital CMOS circuits, the power consumption is mainly due to three current components: (i) the leakage current due to the reverse biased diodes formed between the substrate, the well, and the source and drain diffusion regions of the transistors, (ii) the short circuit current due to the presence of current carrying path from the supply voltage to ground when certain PMOS and NMOS transistors are simultaneously ON for a short period due the signal transitions at the input to the logic gates, and (iii) switching current due to charging and discharging of the load capacitance. Among the three sources of power dissipation, the last component is by far the most. Technology scaling forces a reduction of both VDD (as seen before) and VTH. However VTH scales faster than VDD, and this reduces node by node the distance ($VDD - VTH$). From an intuitive point of view, the distance ($VDD - VTH$) represents the "free" voltage space for analog design. The reduction of this

2 Workflows

A workflow is a depiction of a sequence of Simulation of the various arithmetic circuits was accomplished with HSPICE circuit simulator and by using the Predictive Technology Models (PTM) of CMOS transistors from the Arizona State University [3]. The 32, 45, 65 and 90 nm channel length models were used to investigate the leakage trends within the modeled circuits. Keeping some parameters constant between the circuits ensured the reliability of the collected information. Supply voltage was kept at 1 volt, channel widths at two times the channel length, input waveforms at same frequency and clock signals maintained the same period throughout every test to guarantee that the leakage power consumption test results only showed the effects of the method being tested. Functionality of the circuits was tested and dynamic power consumption simulations were performed. Since the transistor count of each respective circuit did not vary between tests, the well-known

3. Full Adder

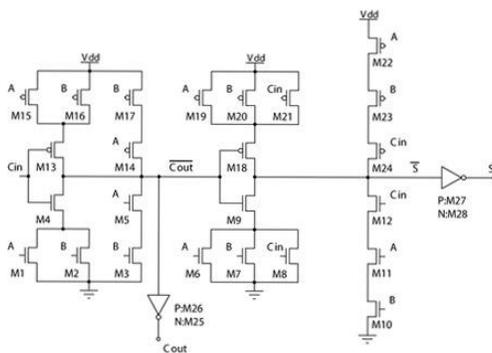


Fig 1: Full adder transistor circuit used for HSPICE simulation [4]

3.1 Dynamic and Leakage Power Consumption

As mentioned earlier, dynamic power consumption of the full adder circuit showed that as feature size increased, so did the dynamic power consumption. Furthermore, as feature size increased, gate thicknesses also increased and leakage power decreased. These trends can be observed below in Fig. 2. In circuits with low transistor count, dynamic power is more significant than leakage power in the circuit's total power consumption.

4 Related Works

The subthreshold leakage is exponentially related to the threshold voltage of the device and threshold voltage changes due to body effect. The source of the nMOS device N1 is connected to ground. Transistor N2 source is connected to drain of N1. The source of N2 is not grounded and it can acquire voltages close to Vdd while its substrate is connected to ground. Therefore the condition $V_{sb}=0$ will not hold in bias cases for transistor N2. The device N1 will experience higher V_{th} due to the difference in the voltage between the source and body. The voltage between drain and source also decreased since the intermediate node has a voltage above the ground resulting reduction in DIBL affect and hence effective saving of leakage power. For turned off the single transistor, leakage current I_{sub0} can be expressed as follows.

$$= A \left(\dots \right) (1 \dots)$$

$$= A \left(\dots \right)$$

$$= A \left(\dots \right) (1 \dots)$$

n =sub-threshold coefficient V =thermal voltage V_{gs0} , V_{th0} , V_{bs0} and V_{ds0} are the gate-to-source voltage, the zero-bias threshold voltage, the base -to-source voltage and the drain-to-source voltage respectively. γ is the body-bias effect coefficient, and θ is the Drain Induced Barrier Lowering (DIBL) coefficient. μ is zero-bias mobility, C_{ox} is the gate-oxide capacitance, W is the width of the transistor, and L_{eff} is the effective channel length. Two transistor are turned off together ($M1=M2$). So,

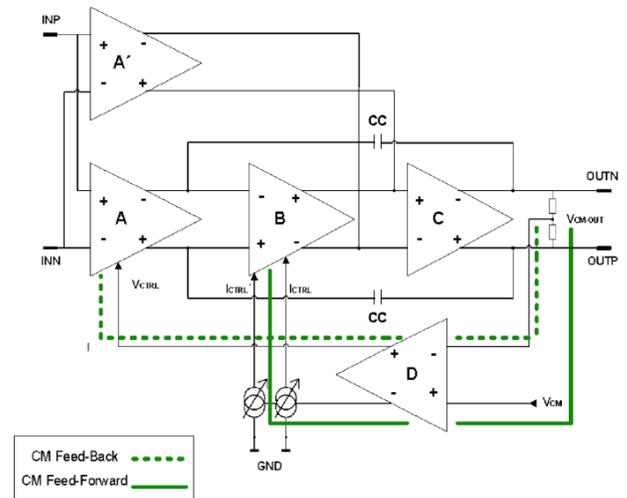


Fig. 2 - Structure of three-stage SMFFC amplifier with the CM-control.

5 Proposed System

The body to source voltage of the sleep transistor is increase in sleep mode to reduce the leakage current. For this in sleepy keeper technique a PMOS and NMOS is added. During sleep mode PMOS is OFF so the body to source voltage of the pull up PMOS is higher than in the active mode. From equation (7), the leakage current decreases as V_{sb1} increases. The body effect, v_{th} also increases due to which performance gets degrade [9]. As shown in fig 12, this technique uses two parallel sleep transistors in pull up network and two parallel sleep transistors in pull down network. For body biasing effect, the source of one of the PMOS sleep transistor is connected to the body of the other PMOS sleep transistor. On the other hand the source of the NMOS sleep transistor is connected to the body of other NMOS sleep transistor. The variable body biasing techniques uses PMOS transistor in GND and NMOS transistor in VDD, both are in paralleled to the sleep transistor for maintaining exact logic state during the sleep mode [9].

Continuous-time analog filters are typically implemented using Gm-C, Active-RC or Active-Gm-RC topologies. The Active-RC and the Active-Gm-RC architectures exhibit a feedback structure and then they could presents a frequency response limitation (limited by the opamp GBW). However they can perform large linear range [16]. On the other hand, At low supply voltage, while Active-RC and ActiveGm-RC can perform rail-to-rail signal processing capability, this is not the case of Gm-C filters, which results extremely inefficient in scaled technologies. As a consequence, closed-loop circuits (like Active-RC and Active- Gm-RC) have then to be considered.

Among them, thanks to the single opamp. Another key problem of both Active-RC and Active-Gm-RC (and any virtual ground based structure) is the bias voltages to be applied at the filter and opamp input and output nodes. The typical approach is to bias input and output nodes at the same voltage level. This however occurs in the bias problem as shown for the differential input stage (that is at the input of

6 Conclusions

In this paper an overview of the challenges imposed by the use of scaled technologies in the analog circuit design is presented. In particular, intrinsic gain decreasing, VDD-V_{TH} reduction and lower supply voltage pushed analog designers to develop new circuit solutions for the analog functional blocks. The case of analog switch, opamp and Active-RC filters is here studied to demonstrate that it is possible to develop new circuit solutions in order to guarantee the same analog performance also in scaled technologies.

7. References

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